3.6.3 Interrupt Control

The I/O control registers, IOCNT0, IOCNT1, and IOCNT2, contain the interrupt control bits. All TMS7000 family members have an IOCNT0 register. Only TMS70x2 and TMS70Cx2 devices have an IOCNT1 register, because they have two more interrupts, INT4 and INT5; only TMS70Cx2 devices have an IOCNT2 register because only they can change the polarity of their external interrupts. The I/O control registers are mapped into PF locations as follows:

Table 3-15. I/O Control Registers

PERIPHERAL FILE	TMS70x0 TMS70Cx0 TMS70CTx0	TMS70x2	TMS70Cx2
IOCNT0	P0	P0	P0
IOCNT1	P16	P16	P2
IOCNT2	N/A	N/A	P1

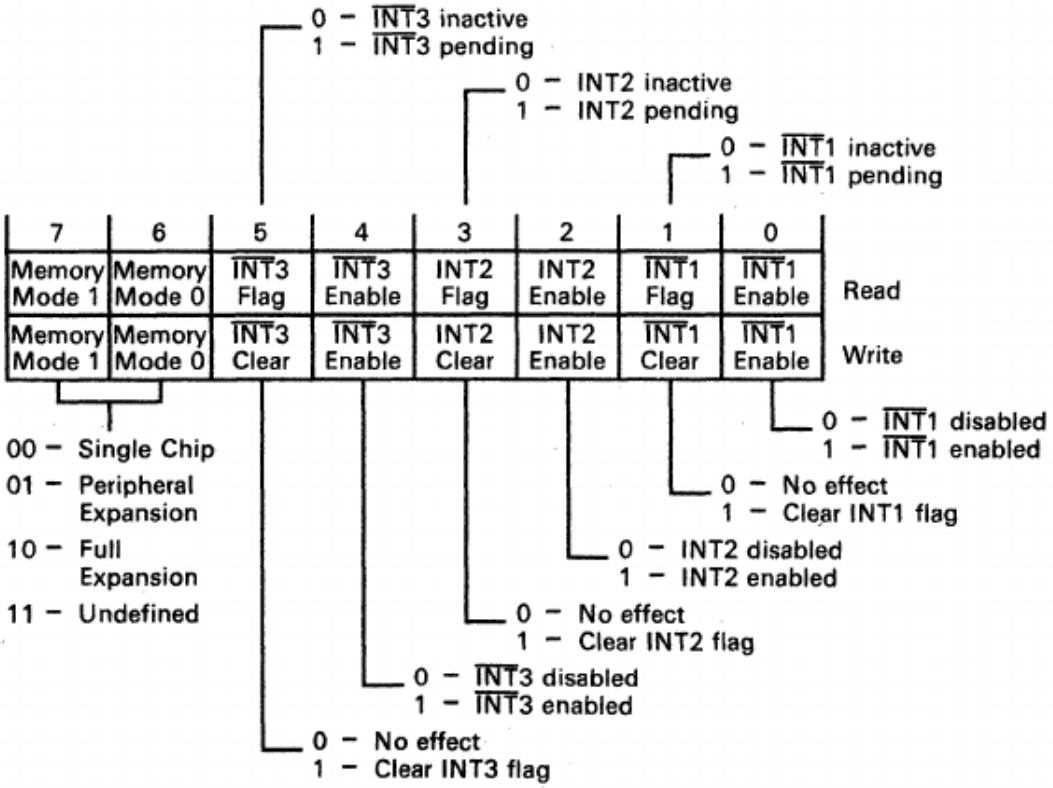


Figure 3-16. IOCNT0 - I/O Control Register 0 (P0 for All Devices)

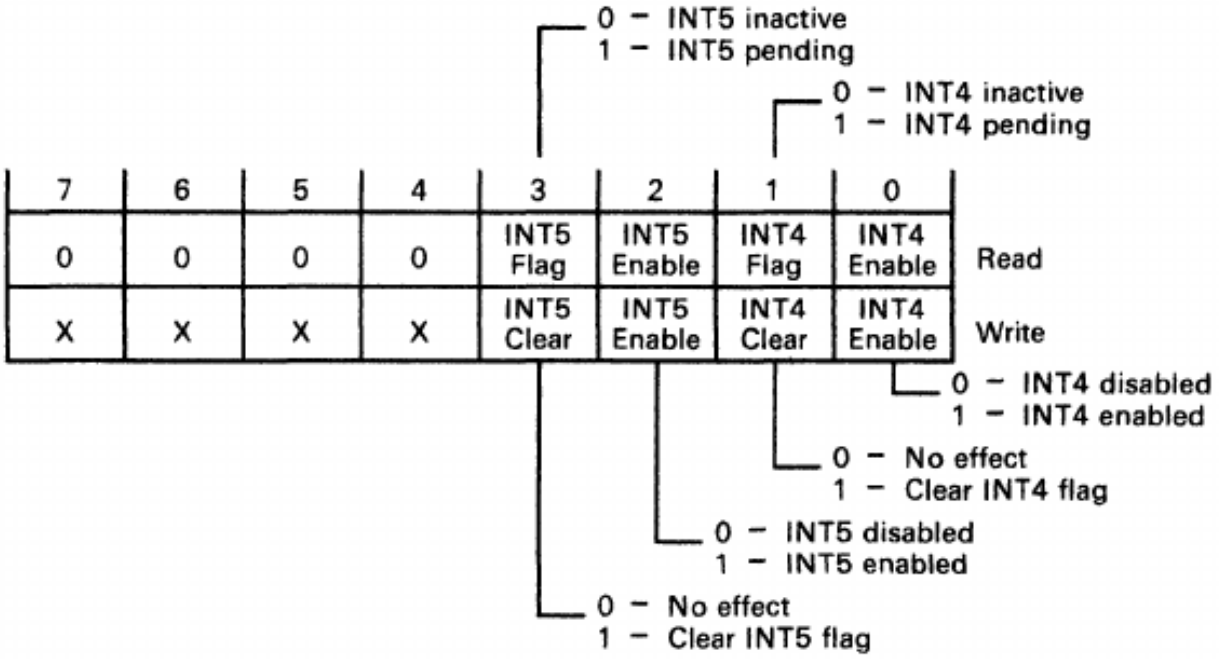


Figure 3-17. IOCNT1 - I/O Control Register 1

In the I/O control registers, each interrupt is associated with a flag bit (INTn flag) and enable bit (INTn enable). The global interrupt enable (I) bit in the Status Register allows all interrupts to be enabled or disabled at the same time. Three conditions must be met before the CPU will recognize an interrupt:

1) A 1 must be written to the INTn enable bit in the IOCNT0 or IOCNT1 register.

2) The global interrupt enable (I) bit in the Status Register must be set to 1 by the EINT instruction.

3) The interrupt must be the highest priority interrupt asserted within an instruction boundary.

Through software, the INTn enable bits can be read and written to:

- Writing a 0 individually masks the corresponding interrupt.
- Writing a 1 allows the interrupt to be recognized.

The reading of the INTn flag is handled differently (see Figure 3-15 on page 3-31):

- An active signal applied to INTn is read as a 1 from one side of an OR gate.
- INTn going active latches a 1 to the other side of the OR gate which stays latched when the signal goes inactive.

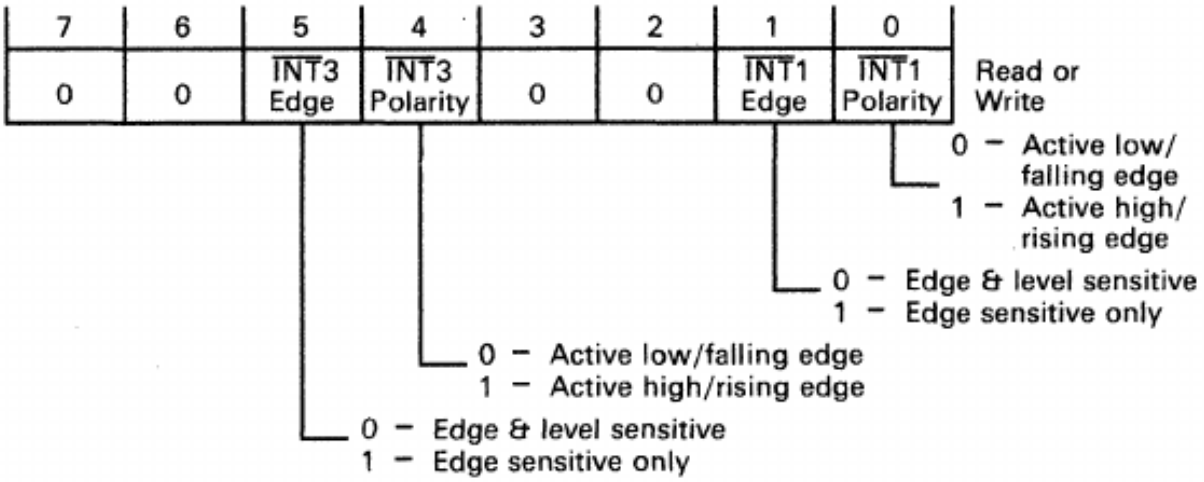


Figure 3-18. IOCNT2 – I/O Control Register 2 (P1 for TMS70Cx2 Only)

Thus, INTn going active is returned both as a latched *and* an edge-sensitive signal for the TMS70x0 and $\overline{\text{INT}}$3 of the TMS70Cx0 devices, while the TMS70Cx2 devices can choose sensitivity via IOCNT2. When a 1 is written to the INTn clear bit, the Pulse flip-flop is cleared. Writing a 0 to the INTn clear bit has no effect.

The INTn flag bit may be tested in software, regardless of whether the interrupt is enabled or disabled. For example, the following program statement waits for the active edge of the interrupt input on the $\overline{\text{INT}}$1 pin by testing INT1 flag:

```
WAIT    BTJZP    %>02,P0,WAIT    Wait for INT1-
*                                (INT1 flag = 1)
```

This allows external interrupt pins to be polled as inputs. Interrupt input pins have an advantage over the other general-purpose inputs if the input signal is a short pulse. The Pulse flip-flop of the interrupt input will always capture a pulse with a width of at least 1.25 × $t_{c(C)}$ cycles, allowing software to detect that the condition occurred, even after the pulse is gone.

Caution:

Due to the read/modify/write nature of the bit manipulation instructions (ANDP, ORP, and XORP), it is possible that the INTn flag bits in the IOCNT0 and IOCNT1 registers could be unintentionally cleared. To avoid these occurrences, *use the MOVP and the STA instructions when writing data to IOCNT0 and IOCNT1*.

Because the INTn flag and INTn clear bits are in the same bit positions, use caution when accessing these bits. For example, you may be able to use XORP to set INT1 enable without altering the state of the INT1 flag (XORP %>03,P0), as long as the INT1 flag does not change state during the instruction execution. However, if a short INT1 pulse sets the Pulse flip-flop between the read and write portions of the instruction execution, a 0 would be read from INT1 flag and a 1 would be written to INT1 clear to reclear INT1 flag. In this case, the $\overline{\text{INT}}$1 pulse would be undetected by the processor. This

same instruction would also affect the INT2 flag and INT3 flag in a similar manner as they are also located in the IOCNT0 register.

Immediately following $\overline{\text{RESET}}$, all interrupts are globally disabled because the I bit (interrupt enable) in the Status Register is reset to 0. Also, the IOCNT0 register is cleared. This clears the INTn enable bits, disabling $\overline{\text{INT}}$1, INT2, and $\overline{\text{INT}}$3 individually and putting the TMS7000 in Single-Chip mode. This does not affect the INTn flag bits from their previous condition before $\overline{\text{RESET}}$. On the TMS70x2 device, a 0 must be written by software to the INTn enable bits in the IOCNT1 register to ensure that INT4 and INT5 are also individually disabled following a $\overline{\text{RESET}}$.

3.7.2 Control Registers for Timer/Event Counters 1 and 2 (TMS70Cx2 Devices)

The control bits and prescaling value of Timers 1 and 2 of the TMS70Cx2 devices are determined by the timer control registers T1CTL0 (P15), T1CTL1 (P14), T2CTL0 (P19), and T2CTL1 (P18). Data can only be written to these control registers, and cannot be read back by a program. When Timer 1 control register T1CTL0 is read, the least significant (LS) byte of the capture latch value associated with Timer 1 is returned. When T1CTL1 is read, the most significant (MS) byte of the Timer 1 readout latch is returned. When T2CTL0 is read, the least significant (LS) byte of the Timer 2 capture latch is returned. When T2CTL1 is read, the most significant (MS) byte of the Timer 2 readout latch is returned. Since the control and prescale bits are write only, the read/modify/write instructions such as ANDP, ORP, and XORP should not be used. The following instructions should be used for timer control-bit manipulations.

```
MOVP    %>XX,Pn          STA   %>01xx
MOVP    A,Pn             STA   *Rn
MOVP    B,Pn             STA   >01xx(B)
```

where:

%XX	=	Immediate 8-bit hexadecimal data value
>01xx	=	16-bit Peripheral-File hexadecimal address
A	=	Register A
B	=	Register B
Pn	=	Peripheral-File register number
Rn	=	General-purpose register pair number

The same instructions are required for writing to the timer data registers, T1LSDATA, T1MSDATA, T2LSDATA, T2MSDATA, and other write-only registers.

3.7.3 Timer Start/Stop (Bit 7) and Capture Latch

Bit 7 of the timer control registers contain a start/stop bit for the timer/event counters.

Bit 7 = 0 A start bit of **0** disables or freezes the timer chain at the current count value.

Bit 7 = 1 A start bit of **1**, regardless of whether the bit was a 0 or a 1 before, loads the prescaler and counter decrementers with the corresponding reload register values, and the timer/event counter operation begins.

3.7.4 Clock Source Control (Bit 6) (See note below.)

For the **TMS70x0, TMS70Cx0, TMS70CTx0,** and **TMS70x2** devices, bit 6 (SOURCE) of T1CTL and T2CTL selects the Timer 1 and Timer 2 clock sources, respectively.

For the **TMS70Cx2** devices, bit 6 (SOURCE) of T1CTL0 and T2CTL0 selects the Timer 1 and Timer 2 clock sources, respectively.

Bit 6 = 0 A source bit of **0** selects the internally generated clock and places the timer/event counter in the Realtime Clock mode using the internal clock source. Each positive transition of the timer clock signal decrements the count chain. Realtime Clock mode allows a program to periodically interrupt and call a service routine, such as a display refresh, by simply setting the prescale reload register and the timer reload register so the routine is called at the desired frequency.

Bit 6 = 1 A source bit of **1** selects the external clock source and places the timer/event counter in the Event-Counter mode. In this mode, each positive transition at the Port A event counter pins decrements the count chain (when the prescaler is decremented to zero, it is reloaded with the prescaler reload register value and the counter is decremented by one).

Summary for all TMS7000 devices (see note below):

	Event Counter Input Pin	**Interrupt Level**
Timer 1	Pin A7/EC1	INT2
Timer 2	Pin A6/EC2	INT5

The Event-Counter mode allows INT2 and INT5 to function as positive edge-triggered external interrupts by loading a start value of 0 into both the prescaler and timer reload register. A positive transition on A7/EC1 or A6/EC2 decrements the corresponding timer through zero and generates an INT2 or INT5. Event-Counter mode can also be used as an externally provided realtime clock if an external clock is input on the I/O pin. The minimum clock period on pins A7/EC1 or A6/EC2 must not be less than $f_{osc}/16$ for TMS70x0, TMS70x2, and TMS70Cx0 devices, or $f_{osc}/4$ for TMS70Cx2 devices. The minimum pulse width of the external signal must not be less than 1.25 state clock cycles [$1.25 \times t_{c(C)}$] to be properly detected by the device.

Note: The TMS70CTx0 devices do not contain an external event counter input pin. Therefore, the clock source must be selected as internal.

3.7.5 Idle/Timer Halt Bit (Bit 5)

The function of the Idle bit (bit 5) in the timer control registers varies depending on the device type.

- **TMS70x0** and **TMS70x2**

  Bit 5 is not used on any of the TMS7000 NMOS devices.

- **TMS70Cx0** and **TMS70CTx0**

  Bit 5 of T1CTL (P3) register is the IDLE bit. This bit selects either of two low-power modes on these devices when the IDLE instruction is executed. (See Section 3.4.2 about CMOS low-power modes.)

  Bit 5 = 0 Wake-Up low-power mode
  Bit 5 = 1 Halt low-power mode

- **TMS70Cx2**

  Bit 5 of the T1CTL0 (P15) and T2CTL0 (P19) registers acts as a timer-halt bit. This bit selects either of two timer operational modes when the IDLE instruction is executed.

  Bit 5 = 0 Timer active mode
  Bit 5 = 1 Halt timer mode

3.7.6 Cascading Timers

The TMS70x2 and TMS70Cx2 devices can have their timers cascaded together to form one large timer. The external clock input for Timer 2 is the Port A pin A6/EC2. This pin can also function as the serial clock I/O line (SCLK) for the serial port on the TMS70x2 devices (see Section 3.8, The Serial Port). Several arrangements are possible with Timer 2 in relation to Timer 3 and the serial port because of this:

- *Both SCLK and Timer 2 clock internal*: the Timer 3 output divided by 2 is driven out of the A6/EC2 pin and Timer 2 is internally clocked by 8 × $t_{c(C)}$.

- *SCLK internal and Timer 2 clock external*: the Timer 3 output divided by 2 is driven out of the A6/EC2 pin and this pin drives the Timer 2 clock. In this mode, Timer 3 and Timer 2 are cascaded together, with Timer 3 driving Timer 2. This is done by setting the Cascade bit to 0 and the Timer 2 source bit to 1. Timer 2 can then be cascaded under software control to either Timer 1 or Timer 3.

- *SCLK external and Timer 2 clock internal*: the input signal drives the serial port clock and Timer 2 is internally clocked by 8 × $t_{c(C)}$.

- *Both SCLK and Timer 2 clock external*: the input signal drives both the serial port clock and Timer 2.

3.7.7 Timer and Prescaler Operation

The timer clock, whether internal or external, is prescaled by a 5-bit modulo-N counter. The prescaling value is determined by the least significant five bits of the timer control register. The timers decrement and an underflow occurs on the transition from 0 to >FF. Thus, a prescale value of >7 will produce an $f_{osc}/128$ clock input into the timer for a TMS70x0 device with a timer clock source of $f_{osc}/16$.

- **TMS70x0, TMS70Cx0, TMS70CTx0** and **TMS70x2**

  Timer 1 Bits 0–4 of Timer 1 control register T1CTL comprise the Timer 1 prescale reload register value.

  Timer 2 Bits 0–4 of Timer 2 control register T2CTL comprise the Timer 2 prescale reload register value. (Available on TMS70x2 only)

- **TMS70Cx2**

  Timer 1 Bits 0–4 of Timer 1 control register T1CTL0 comprise the Timer 1 prescale reload register value.

  Timer 2 Bits 0–4 of Timer 2 control register T2CTL0 comprise the Timer 2 prescale reload register value.

These steps occur during timer operation:

1) Upon starting the timer, the prescaler and timer are loaded from the prescaler reload register and timer reload register, respectively.

2) Each pulse decrements the prescaler by one.

3) When the prescaler countdown decrements through zero, the timer is decremented by one. After the prescaler is decremented,

   If timer ≠ 0 Reload prescaler and go back to step 2.

   If timer = 0 When both the timer and the prescaler decrement through zero together, an interrupt occurs. An INT2 for Timer 1 (INT5 for Timer 2) is momentarily pulsed when both the prescaler and counter decrement past the zero value together. This sets the INT2 or INT5 Pulse flip-flop, as described in Section 3.6.2, Interrupt Operation.

4) The 5-bit prescaler and decrementer are then immediately reloaded with the contents of the prescale reload register and the timer reload register, and the timer will start decrementing with the new reload register values.

- **TMS70Cx2**

  The 16-bit timer reload registers are loaded through the Timer 1 data registers T1LSDATA (P13) and T1MSDATA (P12), and the Timer 2 data registers T2LSDATA (P17) and T2MSDATA (P16). This value is write only. When read, T1LSDATA and T2LSDATA return the current value of the LSB of the Timer 1 and Timer 2 decrementers, respectively, and not the LSB timer reload register value. For this reason, the read/modify/write I/O instructions should not be used to alter the data value in the timer reload registers. T1MSDATA and T2MSDATA will return the value of the MSB readout latch for Timers 1 and 2, respectively. To read the **Timer 1** capture latch, first read T1CTL0 (P15) to obtain the LSB, then read T1CTL1 (P14) to obtain the MSB. To read the **Timer 2** capture latch, first read T2CTL0 (P19) to obtain the LSB, then read T2CTL1 (P18) to obtain the MSB.

3.7.8 Timer Interrupts

When the prescaler and decrementers pass through zero together, an interrupt flag (INTn flag) is set and the prescaler and counter decrementers are immediately and automatically reloaded with the corresponding reload register values. The interrupt levels generated by the timers are INT2 for Timer 1 and INT5 for Timer 2. The period between successive timer interrupts may be calculated by the following formula:

- **TMS70x0, TMS70Cx0, TMS70CTx0** and **TMS70x2**

$$t_{INT} = t_{CLK} \times (PR+1) \times (TR+1)$$

where:

t_{INT} = Period between timer interrupts
t_{CLK} = Period of the timer input clock which is $16/f_{osc}$ for Realtime Clock mode or the period of the external input pin for Event-Counter mode
PR = 5-bit prescaler reload register value
TR = 8-bit timer reload register value

At the falling edge of the $\overline{INT3}$ input, the Timer 1 counter value is loaded into the capture latch. This feature provides the capability to determine when an external event occurred relative to the current Timer 1 decrementer value.

- **TMS70Cx2**

$$t_{INT} = t_{CLK} \times (PR+1) \times (TR+1)$$

where:

t_{INT} = Period between timer interrupts
t_{CLK} = Period of the timer input clock which is $4/f_{osc}$ for Realtime Clock mode or the period of the external input pin for Event-Counter mode
PR = 5-bit prescaler reload register value
TR = 16-bit timer reload register (value written to the MSB and LSB timer reload registers)

On the TMS70Cx2 devices, the falling edge of the $\overline{INT3}$ input will cause the 16-bit decrementer value of Timer 1 to be loaded into the Timer 1 capture latch. Likewise, the falling edge of the $\overline{INT1}$ input will cause the 16-bit decrementer value of Timer 2 to be loaded into the Timer 2 capture latch. This feature provides the capability to determine when an external event occurred relative to the current timer/counter value.

3.7.9 Timer Output Function (TMS70Cx2 Devices)

Timer 1 and Timer 2 have a timer output function which allows the B1 and B0 outputs, respectively, to be toggled every time the timer decrements through zero. This function is enabled by the T1OUT and T2OUT bits (bit 6) in the timer control registers T1CTL1 and T2CTL1.

When operating in the timer output mode, the B0 and/or B1 output cannot be changed by writing to the Port B Data Register. Writing to the appropriate timer's Start bit will reload and start the timer, and will not toggle the output. The output will toggle only when the timer decrements through zero. The timer output feature is independent of INT2 and INT5; therefore, it will operate with INT2 and INT5 enabled or disabled. Also, if the timer is active during the IDLE instruction, the timer output feature will continue to operate.

Whenever the T2OUT or T1OUT bit is returned to 0, B0 or B1 will become an output-only pin, like B2. The value in the B0 or B1 data register will be the last value output by the timer output function, to that B0 or B1 will not change as the T1OUT or T2OUT bit is returned to 0.

Whenever Port B is read, the value on the B0 pin will always be returned, so the current timer output value can be read by reading Port B.

The T1OUT and T2OUT bits are set to 0 by a reset, so the timer output function will not be enabled unless the user sets T1OUT or T2OUT to 1.

The Timer 2 output (T2OUT) cannot be used if Timer 1 and Timer 2 are cascaded together (Cascade bit of T2CTL1 set to 1).

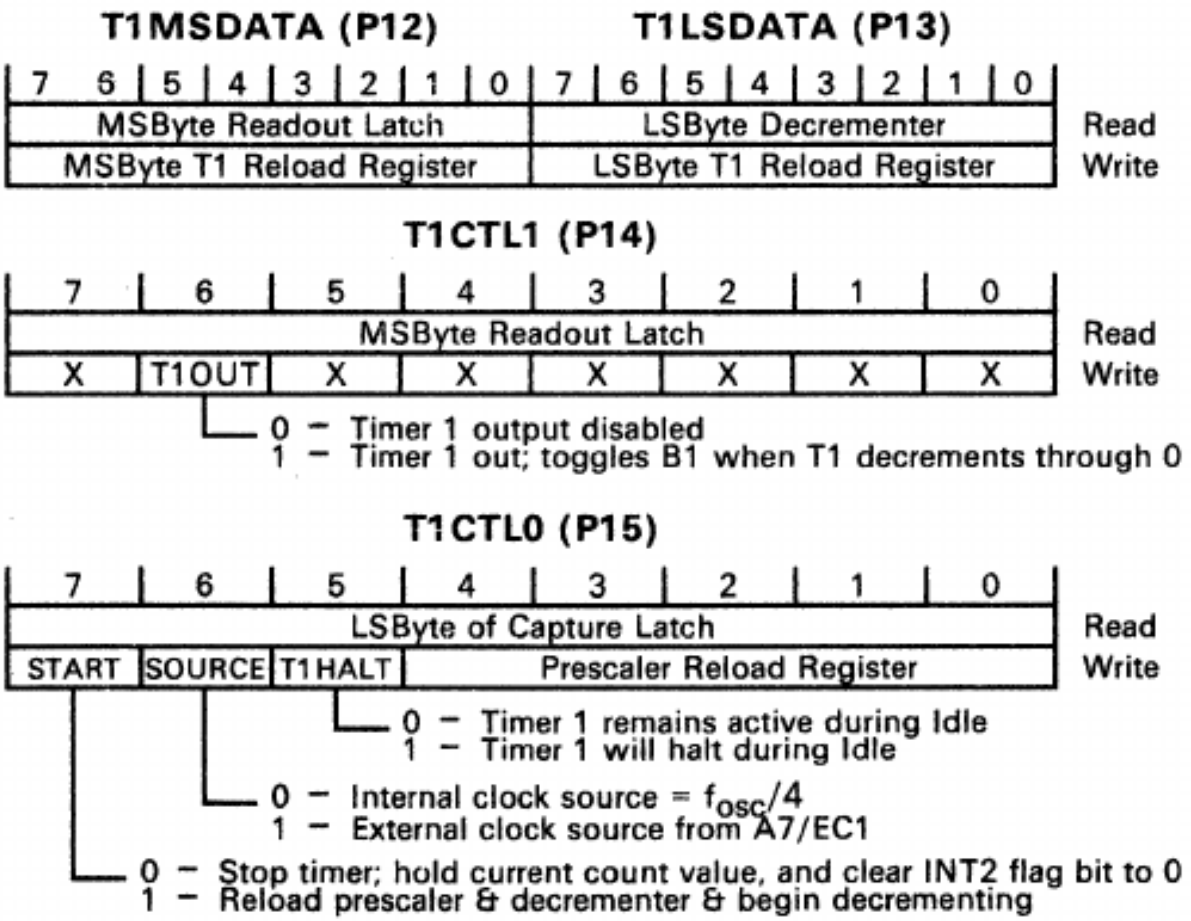


Figure 3-22. Timer 1 Data and Control Registers (TMS70Cx2)

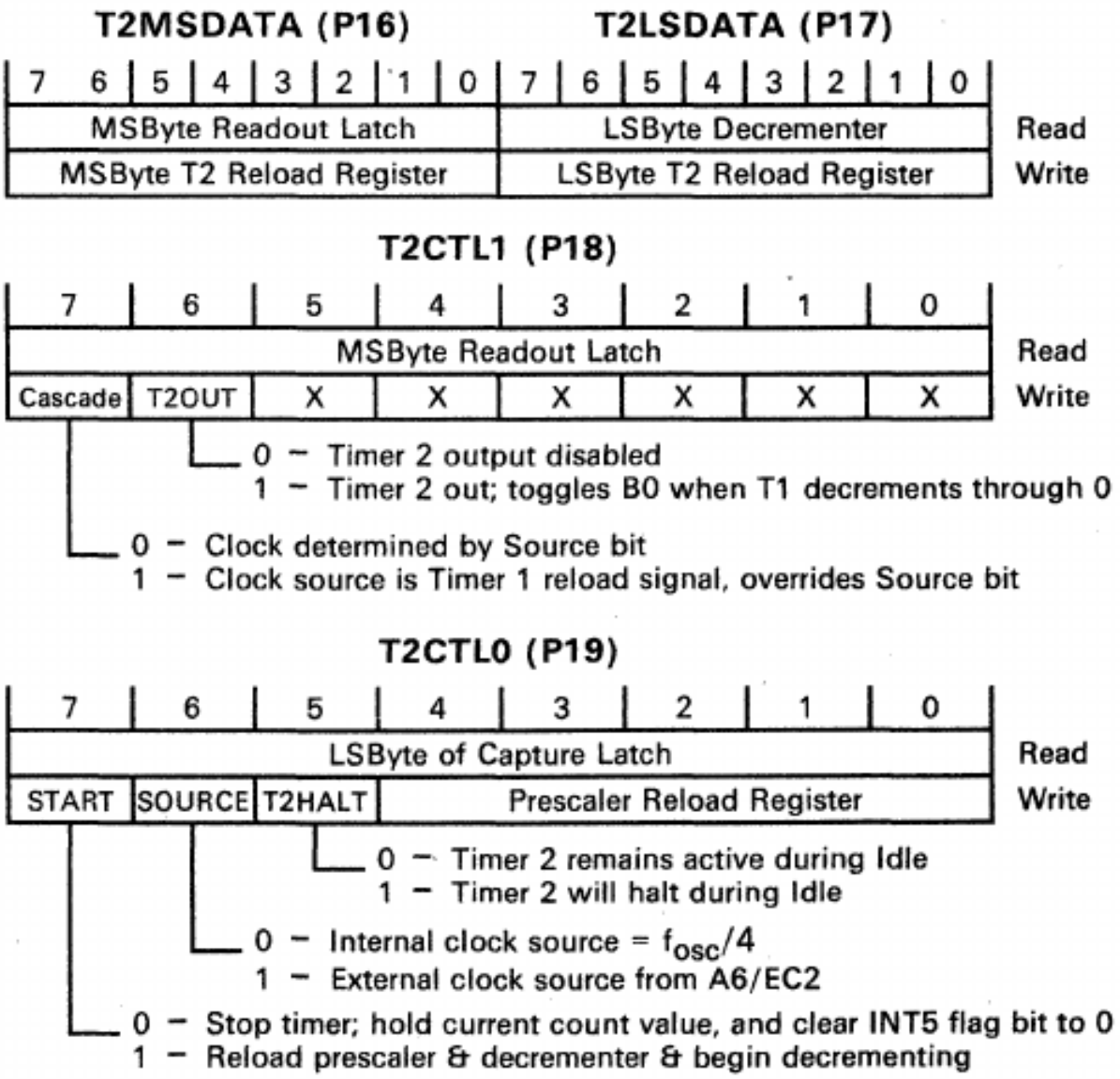


Figure 3-26. Timer 2 Data and Control Registers (TMS70Cx2)

3.8.1 Serial Port Registers

The serial port is controlled and accessed through registers in the Peripheral File. These registers are listed in Table 3-16. Figure 3-27 contains a block diagram of the serial port registers and functional blocks.

Table 3-16. Serial Port Control Registers

REGISTER		NAME	TYPE	FUNCTION
TMS70Cx2	TMS70x2			
P20	P17	SMODE	FIRST WRITE	Serial Port Mode
P21	P17	SCTL0	READ/WRITE†	Serial Port Control 0
P22	P17	SSTAT	READ	Serial Port Status
P23	P20	T3DATA	READ/WRITE	Timer 3 Data
P24	P21	SCTL1	READ/WRITE	Serial Port Control 1
P25	P22	RXBUF	READ	Receiver Buffer
P26	P23	TXBUF	WRITE	Transmission Buffer

† Write only for TMS70x2 devices

The serial mode register, **SMODE**, is the RX/TX control register that describes the character format and type of communication mode (Asynchronous, Isosynchronous, or Serial I/O).

The serial port control 0 register, **SCTL0**, is the RX/TX control register used to control the serial port functions, TX and RX enable, clearing of error flags, and S/W enable.

The serial port Status Register, **SSTAT**, is the read-only serial Status Register used to report the serial port status.

The **T3DATA** register is the read/write Timer 3 data register.

RXBUF is a read-only register containing data from RX. RXBUF is double-buffered with the internal shift register (**RXSHF**) so that the the CPU has at least a full frame to read the received data before RX can overwrite it with new data.

TXBUF is a write-only register from which TX takes the data it transmits. It is double-buffered with the TX shift register (**TXSHF**), so that the CPU has a full frame to write new data before TXBUF becomes empty.

The TXD and RXD lines use I/O pins B3/TXD and A5/RXD, respectively. This configuration allows the TXD and RXD pins to be used as I/O pins if desired. If serial port transmission is disabled, then TXD follows B3. If reception is disabled, then no receiver interrupts occur and A5 functions as an input pin on TMS70x2 devices and as a general-purpose I/O pin on TMS70Cx2 devices. The B3 I/O pin must be set to a 1 in order to enable the TXD pin.

3.8.1.1 Serial Mode Register (SMODE)

The SMODE register is the RX/TX control register that describes the character format and type of communication mode (Asynchronous, Isosynchronous, or Serial I/O).

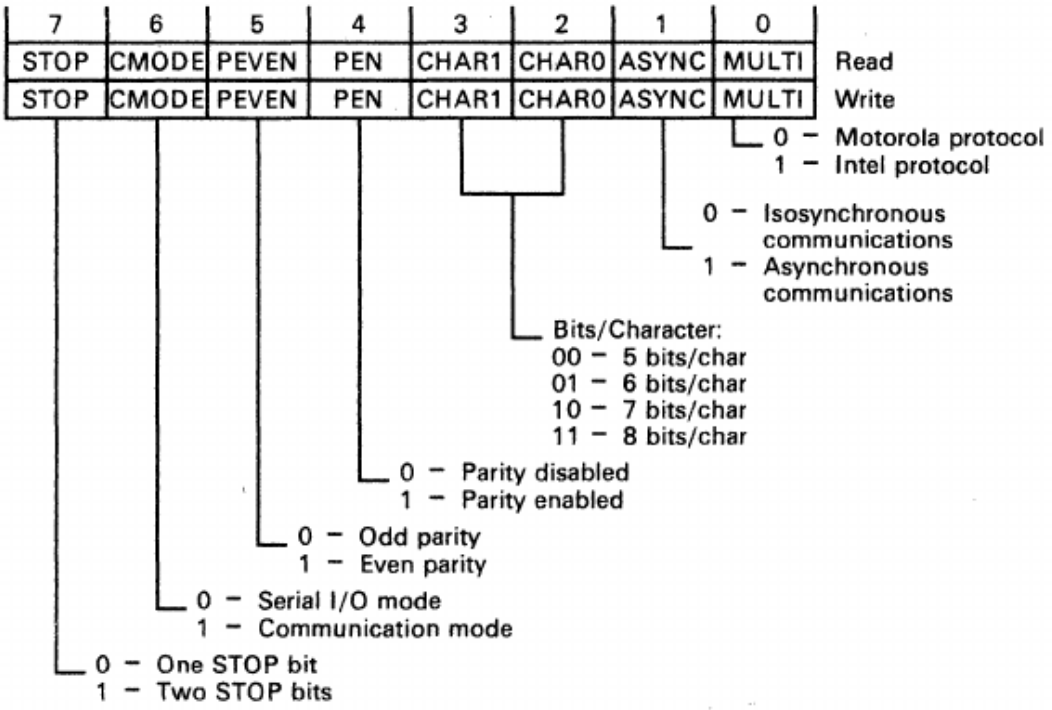


Figure 3-28. Serial Mode Register - SMODE

Multiprocessor Mode (MULTI) Bit 0

There are two possible multiprocessor protocols, Motorola (Section 3.8.3.1) and Intel (Section 3.8.3.2).

0 - Selects the Motorola protocol.
1 - Selects the Intel protocol.

The Motorola mode is typically used for normal communications since the Intel mode adds an extra bit to the frame. The Motorola mode does not add this extra bit and is compatible with RS-232-type communications. Multiprocessor communication is different from the other communication modes because it uses Wake-Up and Sleep functions.

Communications Mode (ASYNC) Bit 1

This bit determines the serial port communication mode.

0 – Selects Isosynchronous mode (Section 3.8.2.2). In this mode, the bit period is equal to the SCLK period; bits are read on a single value basis.
1 – Selects Asynchronous mode (Section 3.8.2.1). In this mode the bit period is 8 times the SCLK period and bits are read on a two out of three majority basis.

Number of Bits per Character (CHAR1, CHAR2) Bits 2,3

Character length is programmable to 5, 6, 7 or 8 bits. Characters less than 8 bits are right-justified in buffers RXBUF and TXBUF and padded with leading zeros. The unused leading bits in TXBUF may be written as don't cares. The RXBUF and TXBUF register formats are illustrated in Figure 3-33 and Figure 3-34.

Parity Enable (PEN) Bit 4

If parity is disabled (PEN set to 0), then no parity bit is generated during transmission or expected during reception. A received parity bit is not transferred to RXBUF with the received data because it is not considered one of the data bits when programming the character field. On the TMS70Cx2 devices, the parity error flag may be set even though parity is disabled.

Parity Even (PEVEN) Bit 5

If PEN is set, then this bit defines odd or even parity according to an odd or even number of 1 bits in both transmitted and received characters.

0 – Sets odd parity.
1 – Sets even parity.

Serial I/O or Communication Mode (CMODE) Bit 6

This bit determines whether the serial port operates in Serial I/O mode or one of the communication modes.

0 – Puts the serial port in Serial I/O mode which allows easy I/O expansion by using external shift registers.
1 – Selects communication mode. The ASYNC bit (bit 1) determines whether the serial port is in Asynchronous or Isosynchronous mode. The MULTI bit (bit 0) determines if the communication uses the Motorola or Intel protocol.

Number of Stop Bits (STOP) Bit 7

This bit determines the number of stop bits sent when the serial port is in Isosynchronous or Asynchronous mode.

0 – Selects one stop bit.
1 – Selects two stop bits. The receiver checks for one stop bit only.

3.8.1.2 *Serial Control Register 0 (SCTL0)*

The SCTL0 register is the RX/TX control register used to control the serial port functions, TX and RX enable, clearing of error flags, and S/W reset. SCTL0 is cleared by a hardware or software reset.

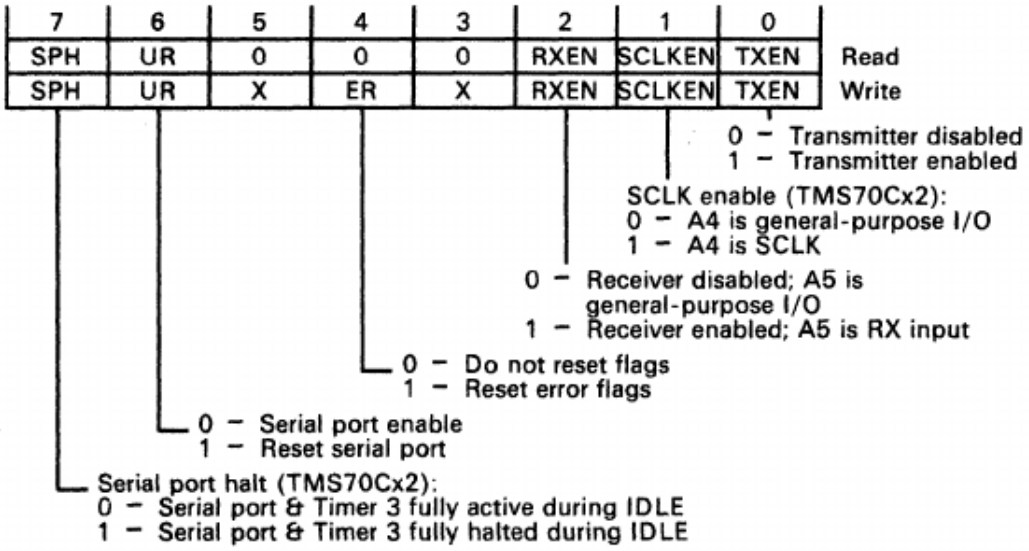


Figure 3-29. Serial Control 0 Register - SCTL0

- **TMS70Cx2**

  SCTL0 is a read/write register, and can be accessed anytime at Peripheral-File location P21.

Transmit Enable (TXEN) Bit 0

Data transmission through TXD (pin B3) cannot take place unless TXEN is set to 1.

When TXEN is reset to 0, transmission does not halt until all the data previously written to TXBUF is sent. Thereafter, B3/TXD can be used as general-purpose output. TXEN is set to 0 by a hardware or software reset.

In Isosynchronous mode, if an internally generated SCLK is used, the SCLK output at pin A6 (TMS70x2) or A4 (TMS70Cx2) is enabled. When the entire frame is transmitted, TX disables SCLK and sets TXRDY and INT4 flag to a 1, and TXEN to 0. TXEN has no direct effect on TXRDY or INT4 flag in this mode.

Serial Clock Enable (SCLKEN) Bit 1 – TMS70Cx2 devices only

This bit determines if the A4/SCLK pin will be used as general-purpose I/O (bit 1 = 0), or as the serial clock SCLK pin (bit 1 = 1).

Receive Enable (RXEN) Bit 2

In the **communication modes** (Asynchronous and Isosynchronous):

0 – Prevents received characters from being transferred into RXBUF, and no RXRDY interrupt is generated. However, the receiver shift register (RXSHF) continues to assemble characters. Thus, if RXEN is set during character reception, the complete character will be transferred into RXBUF.
1 – Enables RX (receiver) to set INT4 flag and enable RXRDY.

In **Serial I/O mode**:

0 – The UR bit sets RXEN to 0.
1 – Enables RX operation.

In Isosynchronous mode, if an internally generated SCLK is used, the SCLK output at pin A6 (TMS70x2) or A4 (TMS70Cx2) is enabled. When the entire frame is received, RX disables SCLK and sets RXRDY and INT4 flag to a 1, and RXEN to 0. RXEN has no direct effect on RXRDY or INT4 flag in this mode.

Error Reset (ER) Bit 4

The error reset bit is used to reset any error flags during serial port operation.

0 – No error flags are affected.
1 – Clears all three error flags in the SSTAT register (PE, OE, FE).

Software UART Reset (UR) Bit 6

Writing a 1 to this bit puts the serial port in the reset condition, enabling the SMODE register for initialization. SCLK (pin A6 on TMS70x2 devices, pin A4 on TMS70Cx2 devices) is put in the high-impedance input state. The TXD signal is held at 1 so the B3 pin may be used as a general-purpose output line. On TMS70Cx2 devices, the A5/RXD signal becomes a general-purpose I/O line; on TMS70x2 devices, it becomes an input.

Until a 0 is written to UR, all affected logic is held in the reset state. UR must be set to 0 before the CPU can write a 1 to CLK and output SCLK on Port A. UR is set to 1 by hardware $\overline{\text{RESET}}$. The UART reset affects only the items above; it is not a general device reset like the $\overline{\text{RESET}}$ pin.

Serial Port Halt Enable (SPH) Bit 7 – TMS70Cx2 devices only

This bit determines if the serial port and Timer 3 will be active or not during an IDLE instruction.

0 – Serial port and Timer 3 will be fully active during an IDLE instruction.
1 – Serial port and Timer 3 will be halted during an IDLE instruction.

3.8.1.3 *Serial Port Status Register (SSTAT)*

SSTAT is the read-only serial port Status Register. Bits 0, 1, and 6 of this register are cleared by a hardware or software reset.

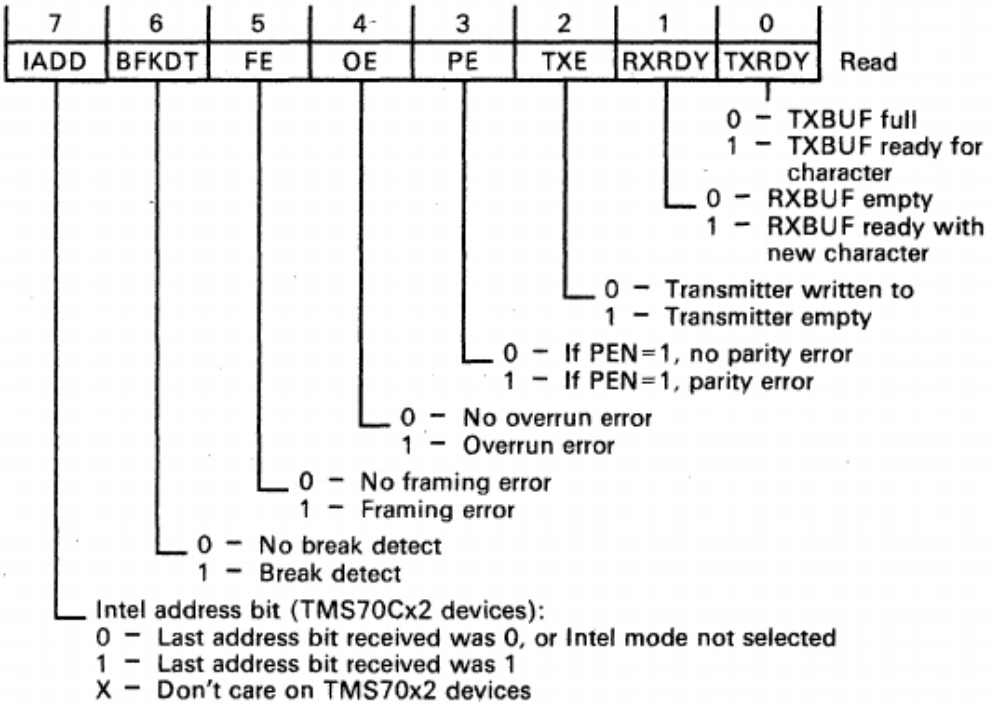


Figure 3-30. Serial Port Status Register – SSTAT

- **TMS70x2**

  The SSTAT register is accessed anytime by reading Peripheral-File location P17.

- **TMS70Cx2**

  The SSTAT register is accessed anytime by reading Peripheral-File location P22.

Transmitter Ready (TXRDY) Bit 0

The TXRDY bit is set by the transmitter to indicate that TXBUF is ready to receive another character. It is automatically reset when a character is loaded. If the serial port interrupt (INT4) is enabled, it is issued at the same time the TXRDY bit is set. Resetting the UART sets TXRDY to 1.

Receiver Ready (RXRDY) Bit 1

This bit is set by the receiver to indicate that RXBUF is ready with a new character. It is automatically reset when the character is read out. If the serial port interrupt (INT4) is enabled, it is set at the same time that the RXRDY bit is set. Resetting the UART sets RXRDY to 1.

Transmitter Empty (TXE) Bit 2

The TXE bit is set to 1 when the transmitter shift register (TXSHF) and TXBUF (shown in Figure 3-34, page 3-62) are empty. It is reset to 0 when the TXBUF is written to. Resetting the UART sets TXE to 1.

Parity Error (PE) Bit 3

PE is set when a character is received with a mismatch between the number of 1s and its parity bit. This bit is reset by the ER bit in SCTL0. Disabling the parity does not disable this flag, so this flag may be set even when the parity is disabled.

Overrun Error (OE) Bit 4

OE is set when a character is transferred into RXBUF (shown in Figure 3-34) before the previous character has been read out. The previous character is overwritten and lost. OE is reset by the ER bit in SCTL0.

Framing Error (FE) Bit 5

FE is set when a character is received with a 0 stop bit, meaning that synchronization with the start bit has been lost and the character is incorrectly framed. The ER bit in SCTL0 resets FE.

Break Detect (BRKDT) Bit 6

The BRKDT bit shows that a break condition has occurred. BRKDT is set if the RXD line remains continuously low for 10 bits or more, starting from the end of a frame (stop bit). When the break ends, BRKDT is set to a 0 immediately. In the Serial I/O mode, BRKDT remains a 0. UR (SCTL0 bit 6) sets BRKDT to 0. A break is generated by setting Port B bit 3 low. Setting B3 high again resumes TXD operation.

The TXD and RXD lines are multiplexed on I/O lines B3 and A5, respectively. This configuration allows the TXD and RXD pins to be used as I/O pins if desired. If transmission is disabled, then TXD follows B3. If reception is disabled, then no receiver interrupts occur and A5 is an input bit.

Intel Address Bit (IADD) Bit 7 – TMS70Cx2 devices only

This bit shows the last data bit received when using the Intel protocol.

0 – Last address bit received was 0, or Intel mode was not selected.
1 – Last address bit received was 1.
X – Don't care on TMS70x2 devices.

3.8.1.4 *Serial Control Register 1 (SCTL1)*

The SCTL1 register is the read/write serial control register 1. It is used to control the Timer 3 start/stop function, the source of SCLK, multiprocessor communication, Timer 3 interrupt, and the Timer 3 prescaler value.

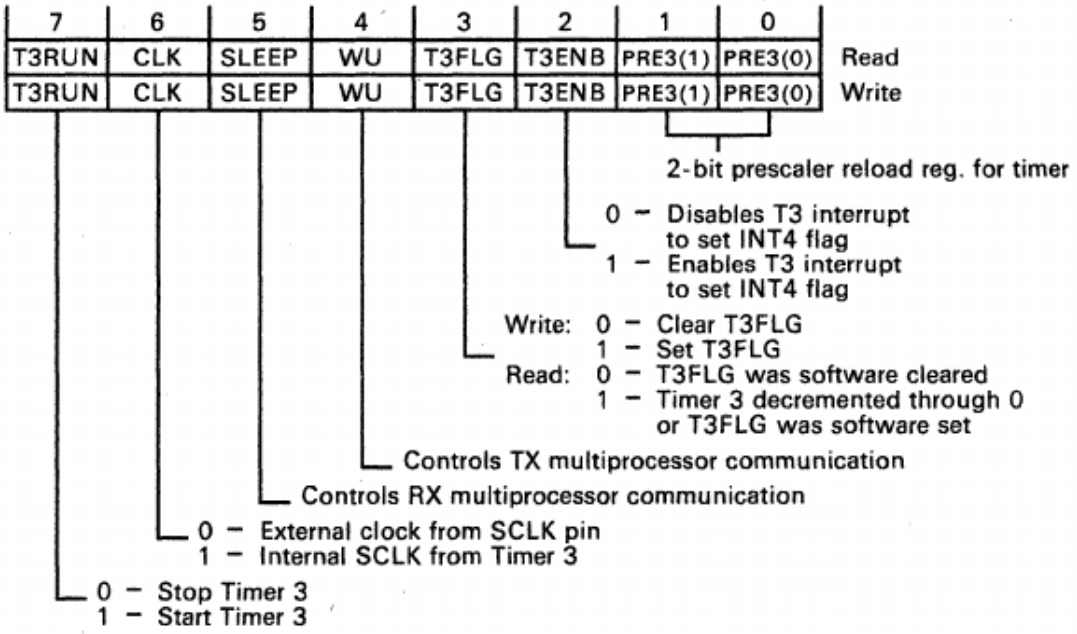


Figure 3-31. Serial Port Control 1 Register – SCTL1

- **TMS70x2**

  The SCTL1 register is accessed at Peripheral-File location P21.

- **TMS70Cx2**

  The SCTL1 register is accessed at Peripheral-File location P24.

Timer 3 Prescale Reload Register (PRE3(1), PRE3(0)) Bits 0,1

These are the prescale bits for Timer 3. The internal clock input to Timer 3 is either f_{osc}/4, /8, /16, or /32, depending on how the prescale bits are set. The Timer 3 output divided by 2 is the actual baud rate for the Isosynchronous mode; divided by 8, it is the baud rate for for the Asynchronous mode.

Timer 3 Interrupt Enable (T3ENB) Bit 2

When T3ENB is set to 1, Timer 3 sets INT4FLG to 1 when it sets T3FLG to 1. T3ENB is reset to 0 by a hardware reset, but not by UR (SCTL0 bit 6). This allows Timer 3 to operate independently of the serial port.

3.8.1.6 *Receiver Buffer*

The receiver buffer, RXBUF, is a read-only register used to store the current RX data. Writing has no direct effect on this register. Data in the RXBUF is right justified, padded with leading 0s.

7	6	5	4	3	2	1	0
MSb			Receiver Data				LSb
0	0	0	←	5 Data Bits			→
0	0	←	6 Data Bits				→
0	←	7 Data Bits					→
←	8 Data Bits						→

Figure 3-33. Receive Buffer – RXBUF

- **TMS70x2**

  The read-only RXBUF register is accessed at PF location P22.

- **TMS70Cx2**

  The read-only RXBUF register is accessed at PF location P25.

3.8.1.7 *Transmitter Buffer*

The transmitter buffer, TXBUF, is a write-only register used to store data bits to be transmitted by TX. Data written to TXBUF must be right justified because the left-most bits will be ignored for characters less than eight bits long.

7	6	5	4	3	2	1	0
MSb			Transmitter Data				LSb
X	X	X	←	5 Data Bits			→
X	X	←	6 Data Bits				→
X	←	7 Data Bits					→
←	8 Data Bits						→

Figure 3-34. Transmitter Buffer – TXBUF

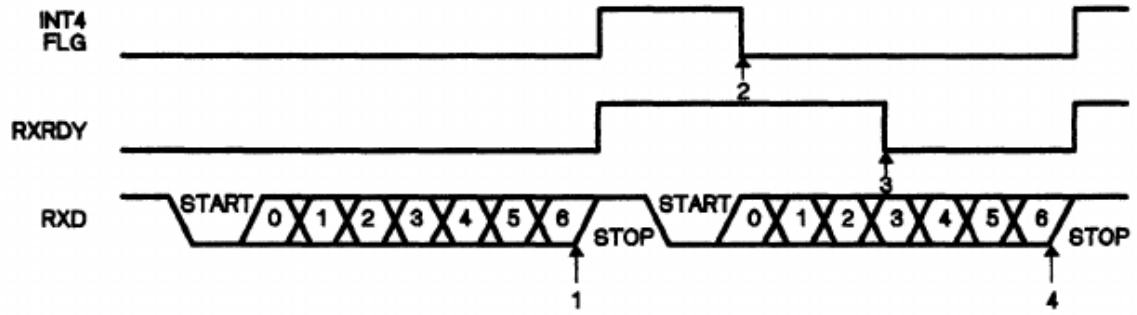
- **TMS70x2**

  The write-only TXBUF register is accessed at PF location P23.

- **TMS70Cx2**

  The write-only TXBUF register is accessed at PF location P26.

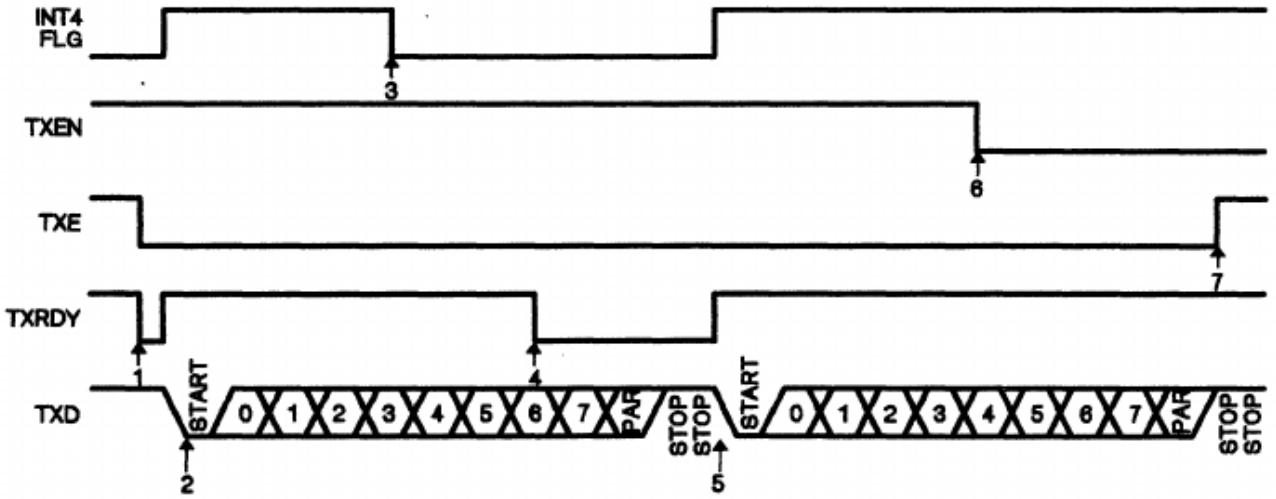
3.8.1.8 RX Signals in Communication Modes



Notes: 1) Format shown is start bit + seven data bits + stop bit.
2) SCLK is continuous, external or internal.
3) If RXEN = 0, RXSHF still receives data from RXD. However, the data is not transferred to RXBUF and RXRDY and INT4FLG are not set.

Sequence of Events:
1) RXSHF data is transferred to RXBUF. Error status bits are set if an error is detected.
2) Software writes to INT4CLR to clear INT4FLG. If not, CPU clears.
3) INT4FLG on entry to level 4 interrupt routine.
4) Software reads RXBUF.

3.8.1.9 TX Signals in Communication Modes



Notes: 1 Format shown is start bit + eight data bits + parity bit + two stop bits.
2) SCLK is continuous whether internal or external.

Sequence of Events:
1) Software writes to TXBUF.
2) TXBUF and WU data are transferred to TXSHF and WUT. INT4FLG and TXRDY are set.
3) Software writes to INT4CLR to clear INT4FLG or CPU clears INT4FLG on entry to level 4 interrupt routine.
4) Software writes to TXBUF.
5) Software writes to INT4CLR to clear INT4FLG or CPU clears INT4FLG on entry to level 4 interrupt routine.
6) Software resets TXEN; current frame will finish and transmission will stop whether TXBUF is full or empty.
7) TXE is set if TXBUF and TXSFT are empty.

3.8.4 Serial Port Initialization

The serial port must be initialized before it can be used; then it may be operated by simply reading and writing to Peripheral-File registers. A good programming practice is not to assume that any registers have particular values at power-up or reset. A program should write to every value or register that might affect the serial port. Initialize the serial port as follows:

- **TMS70Cx2**

  1) Set B3 data value to 1. This allows the TXD line to transmit.

  2) Write to the SMODE register (P20). This sets the character format and the type of communication mode.

  3) Write to the SCTL0 register (P21). Enable the receiver or the transmitter or both. The UR bit must be set to 0.

  4) Load the Timer 3 reload register value (P23).

  5) Write to SCTL1 register (P24) to initialize Timer 3, the clock source, and multiprocessor mode, if desired.

  Once the serial port is initialized it can be operated continuously in the selected operational mode. To send data, simply write to the transmit buffers (P26), making sure that the transmitter is enabled (P21). Take input data from the receive buffer (P25) with the receiver enabled (P21). If the mode must be changed, the serial port must be reset and then re-initialized for the desired mode. The serial port can be reset in three ways: hardware reset (via the RESET pin) or software reset (via the UR bit in SCTL0), or by writing to the SMODE register.