Trademark Acknowledgments

CP/M (R) is a registered trademark of Digital Research, Inc.
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NOTE

What is refered to throughout this manual as PINE is the same as HX-40 or PX-4, which are the same but have different names depending upon the market.

NOTICE

PX-4·HX-40

Operating System Reference Manual

EPSON

INTRODUCTION

1.1 Purpose of This Manual

This manual describes the functions of the operating system for the EPSON PINE microcomputer system. It is intended for system house users who are to develop applications programs which make the best of the PINE's capabilities.

The reader is assumed to be familiar with the following:

- Basic knowledge about the CP/M operating system
- General knowledge about machine-language programming
- Z80 instructions

1.2 Before Reading This Manual

This manual uses the following notational conventions:

1.2.1 Data representation

This manual uses binary, decimal, and hexadecimal numbers. They are represented in the formats:

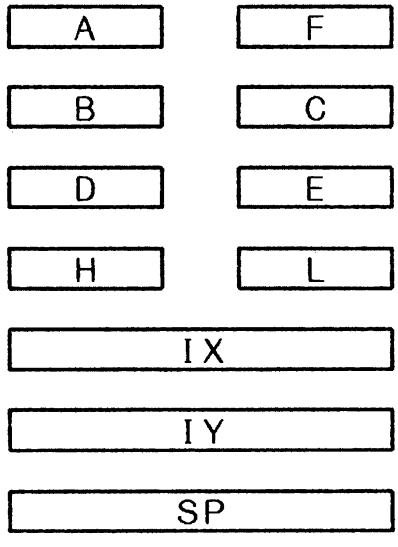
Binary: 00100011B (Numbers are followed by 'B')
Decimal: 35 (only numerals)
Hexadecimal: 23H (Numbers are followed by 'H')

Character constants are enclosed in apostrophes (').
Example:

```
'ABC'
```

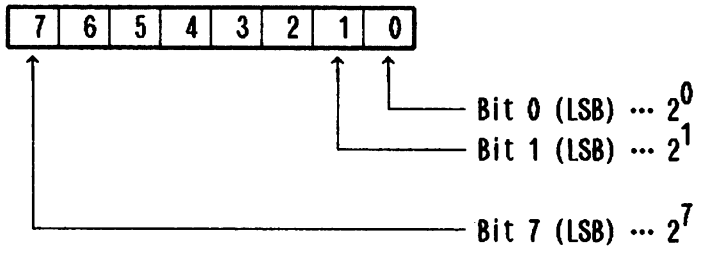
1.2.2 Register Representation

The PINE registers are illustrated below.



Registers are expressed as A, B, DE, HL, and so on. They may sometimes be followed by the word "register" to clearly identify them. The bits of the F (flag) register are sometimes identified as the Z flag (or Z), the C flag (or C), and so on.

1.2.3 Bit Representation
Bits are numbered Ø, 1, and so on, from the lowest order bit (Ø) to the highest order bit. The lowest order bit is referred to as the least significant bit (LSB) and the highest order bit as the most significant bit (MSB).



1.2.4 Address Representation
Addresses are generally represented in hexadecimal notation. I/O addresses are prefixed by "P".
Examples:

ØØ1ØH	Memory address 1ØH
P1ØH	I/O port address 1ØH

Note that the contents of I/O addresses may differ during read and write operations.

1.2.5 Operating System Types
The PINE runs under three types of operating systems (OS) :
Kana OS V1.Ø (Japan only)
Kana OS V2.Ø (Japan only)
Export version OS V1.Ø
These operating systems differ only in the characters they support. This manual will explain about Export version OS V1.Ø

1.2.6 Organization of This Manual
This manual is divided into Part I, Part II, Part III and Part IV. Part I, "Firmware," explains the PINE firmware, Part II, "Software," describes the PINE CP/M operating system, Part III, "INTERFACE" explains the PINE firmware, and Part IV, "BASIC" describes the PINE Basic.

PART I FIRMWARE

PART II SOFTWARE

PART III INTERFACE

PART IV BASIC

Part I FIRMWARE

CONTENTS (FIRMWARE)

CHAPTER 1 GENERAL DESCRIPTION

CHAPTER 1 GENERAL DESCRIPTION

1.1 PINE System Configuration

1.1.1 General

The PINE is centered on a C-MOS Z-80-compatible microprocessor. Its main memory consists of 64K bytes of RAM and up to 96K bytes of ROM. These RAM and ROM are used alternatively using a bank switching technique.

The PINE also has a 4-bit C-MOS 7508 processor, as its slave CPU, which is used to control the keyboard, clock, and power units. In addition to these processors, the PINE employs three types of semicustome gate array (GA) ICs, namely, the main memory control GA, interrupt controller GA, and I/O control GA.

Power to the PINE is supplied from the NiCd power battery, Mn dry batteries, or AC adapter.

Figure 1.1.1 shows the PINE hardware configuration.

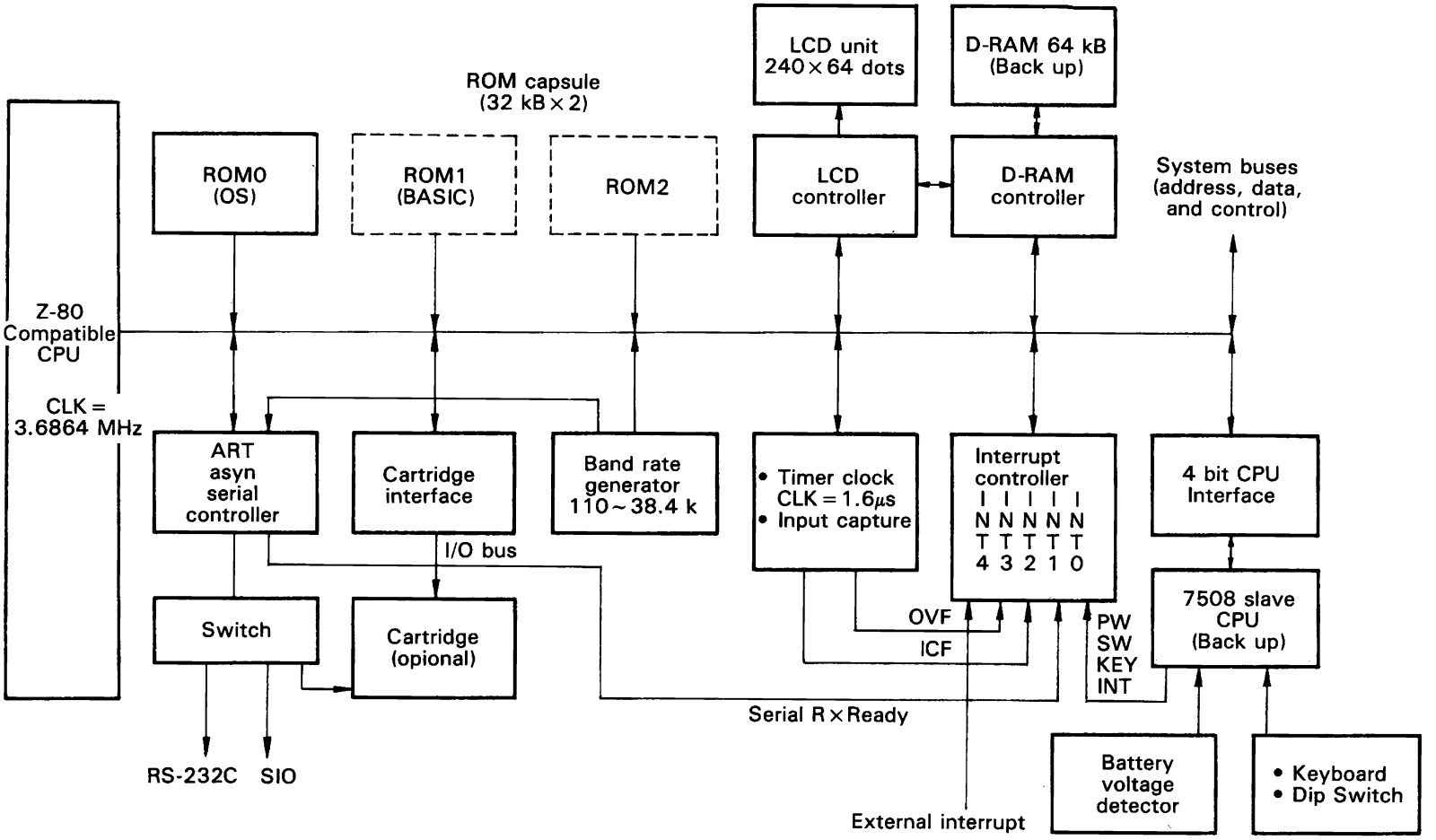


Figure 1.1.1 Hardware Configuration

1.1.2 Hardware Description

1.1.2.1 CPU

The PINE main CPU is a Z-80-compatible C-MOS CPU uPD70008 running at a basic clock rate of 3.6864 MHz. The CPU is put into the sleep state by the HALT instruction to save power energy.

1.1.2.2 Main memory

ROM: 96K bytes (maximum): 256K-bit C-MOS mask ROM x 3
RAM: 64K bytes: 64K-bit C-MOS D-RAM x 8
Memory reads, writes, and refreshing are controlled by the D-RAM controller GA. The RAM memory is battery backed up and its data is sustained even when power switch is turned off.

1.1.2.3 7508 (slave CPU)

The slave CPU is a 4-bit C-MOS 7508 microprocessor equipped with the sleep and timer functions. It runs on a basic clock of approximately 270k Hz. The 7508 is battery backed up and can continue its operation even when power is shut down. The 7508 is used to monitor the battery voltage and temperature. Its primary functions are to:

- Provide the timer/clock functions.
- Sense D-RAM temperature (at power-off time)
- Turn power on and off.
- Set and reset the system.

1.1.2.4 GAPNDL (Main memory control GA)

The GAPNDL controls the operations (read, write, and refresh) of the 64K-byte DRAMs as well as the 240 x 64 dots LCD unit.

1.1.2.5 GAPNIT (Interrupt/timer control GA)

The GAPNIT serves as:

- Interrupt controller
- Timer/baud rate generator (with input capture feature)
- Interface to the 4-bit 7508 CPU
- ROM/DRAM address decoder and DRAM address multiplexer

1.1.2.6 GAPNIO (I/O control GA)

The GAPNIO serves as:

- Asynchronous Receiver Transmitter (ART)
- Centronics interface
- Cartridge (CTG) interface
- Serial I/O interface (SIO)
- RS-232C interface
- LED and buzzer interface

1.1.2.7 SIO Interface

The SIO interface specifications are given below.

Level:	RS-232C level ±5 V
Baud rates	110, 150, 200, 300, 600, 1,200, 2,400, 4,800, 9,600, 19,200, 38,400, 75 bps
Start bits:	1 bit
Stop bits:	1 or 2 bits
Parity:	Even/odd or no parity
Communication mode:	Full duplex
Error checking:	Parity, framing, and overrun errors

The ART in the GAPNIO is used.

1.1.2.8 RS-232C Interface

The RS-232C interface specifications are given below.

Level:	RS-232C level +5 V
Baud rates:	Same as for SIO.
Start bits:	Same as for SIO.
Stop bits:	Same as for SIO.
Parity:	Same as for SIO.
Communication mode:	Same as for SIO.
Error checking:	Same as for SIO.

The ART in the GAPNIO is used.

1.1.2.9 Keyboard

There are two types of keyboards for the PINE: standard and item keyboards.

Standard keyboard:	72 keys (66 keys plus 6 switches)
Item keyboard:	58 keys (55 keys plus 3 switches)
Contact type:	Mechanical contacts
Features:	N-key rollover and auto-repeat features Programmable repeat interval 7-character buffer Stop-key only mode

1.1.2.10 LCD

The PINE is provided with a 1/64-duty, 240 x 64 dot matrix LCD unit. The LCD drivers are:

X:	SED 1120 x 4
Y:	SED 1130 x 1
Drive voltage:	10 to 18 volts; view angle is adjustable with a potentiometer.
VRAM area:	2K bytes
Display mode:	Dot image (no character generator)
Scrolling:	Vertical dot scrolling

1.1.2.11 Buzzer

The PINE has a piezo-electric buzzer. The buzzer input is obtained by ORing the audio signal from the cartridge interface with the SP signal from the CPU. The buzzer is disconnected when an ear plug is plugged into the external loudspeaker jack.

1.1.2.12 ROM capsule

The PINE can accommodate either 8K-, 16K-, or 32K-byte ROM (maskable or programmable) capsules. These ROM devices have different pin assignments as listed below.

ROM / Pins	61364	613128	613256	27C64	27C256
27pin	OE1*	OE1*	A14	$\overline{PGM}$	A14
26pin	OE2*	A13	A13	Nc	A13
22pin	OE0*	OE0*	OE0	$\overline{OE}$	$\overline{OE}$
20pin	CS*	CS*	CS*	$\overline{CS}$	$\overline{CS}$
	Maskable			P-ROM	

Asterisks identify mask-programmable ROMs.

OE0* and CS* must be active low. For 61364, *E1* must be active high and *E2* must be active low. For 613128, OE1* is don't care or must be active low. When OE1* is set to active low, jumper J4 or J5 to side B.

1.2 Address Map

The PINE has four types of memory:
1) DRAM (64K bytes)
2) ROM1
3) ROM2
4) ROM3
5) External memory

DRAMs make up a 46K bytes of system RAM memory and are controlled by gate array GAPNDL. ROM1 is used to store the operating system and ROM2 and ROM3 to store application programs. Both have a maximum capacity of 32K bytes (may also be used as 16K- or 8K-byte ROM). The external memory refers to the memory which is installed in the external expansion box and connected to the main unit through the system bus. The main unit does not know whether it is made up of ROM or RAM devices.

A 4-bit bank switch (BANKR bits 7-4 for BANKØ through BANK3) is provided for memory management. This switch is used in conjunction with the address inputs to address the memory. Figure 1.2.1 shows the relationship between BANK3 through BANKØ and their address spaces.

The memory devices installed in the main unit are all controlled by gate array GAPNIT. GAPNIT issues a Select (enable) signal to the memory in the main unit when $\overline{\text{MEN}}$ from the external expansion box is Ø and disables the main unit memory when $\overline{\text{MEN}}$ is 1.

$\overline{\text{MEN}}$ is held at the Ø level when no external expansion box is installed. If an external expansion box is installed, all memory is controlled by the external expansion box.

The external expansion box a bank signal for memory management (different from those generated by GAPNIT and assigned a 1-level higher priority) which is used with the address inputs to determine whether the main unit memory or external memory is to be used.

When using the main unit memory, the external expansion box sets $\overline{\text{MEN}}$ to Ø to disable the external memory and leaves the main memory addressing to GAPNIT's control. When using the external memory, it sets $\overline{\text{MEN}}$ high to disable the memory in the main unit. The GAPNIT does nothing for external memory addressing.

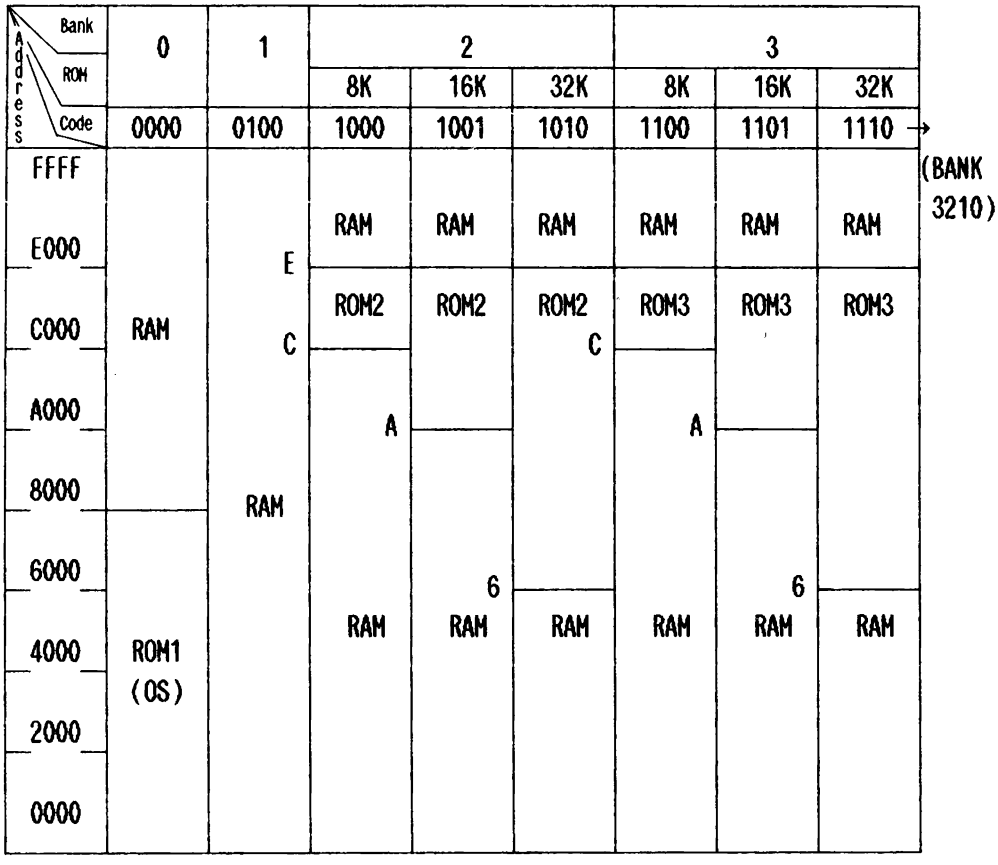
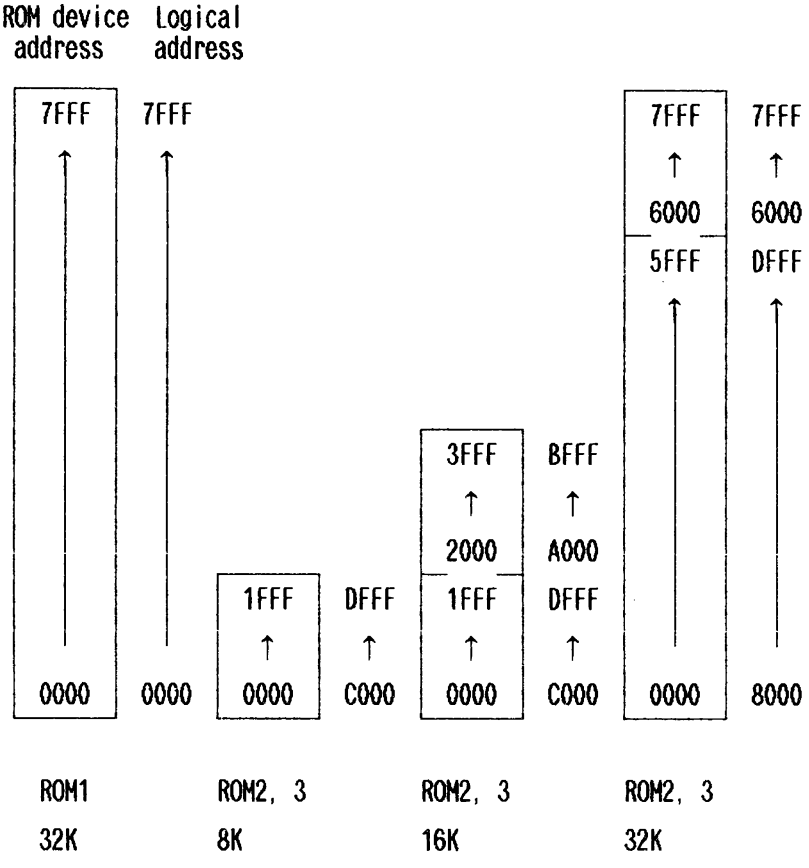


Fig. 1.2.1 PINE Memory Map

Note: Note the relationship between the logical and physical ROM addresses when programming ROM devices.



* See also the figure on the previous page.

1.3 I/O Map

1.3.1 Introduction

The PINE I/O addresses space is allocated to the three gate array LSIs (i.e., GAPNIT, GAPNDL, and GPNIO) and the I/O devices in the external expansion box. The GAPNIT are assigned I/O addresses P00H through P07H, the GAPNDL is assigned P08H through P0FH, the GAPNIO is assigned P10H through P1FH, and the external I/O devices P20H through PFFH.

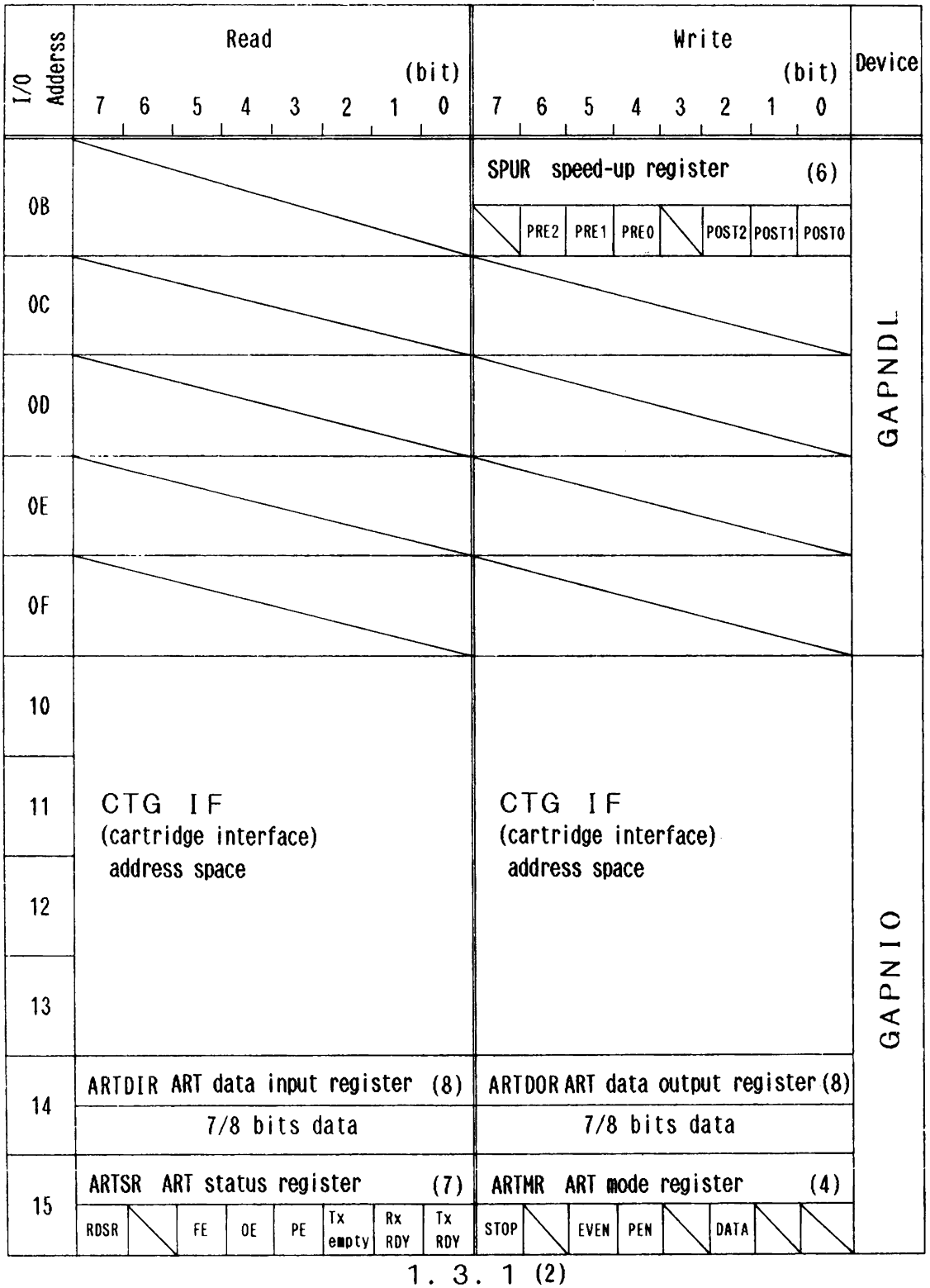
1.3.2 I/O Address Space

Table 1.3.1 lists the I/O addresses assigned to the PINE. In the table, I/O address bits identified by an asterisk (EDJ and ECA) are used only for development boards and valid only for board development. The unused I/O addresses between P00H through P1FH must not be used by the user. Any accesses to inhibited I/O address may cause computer malfunctions.

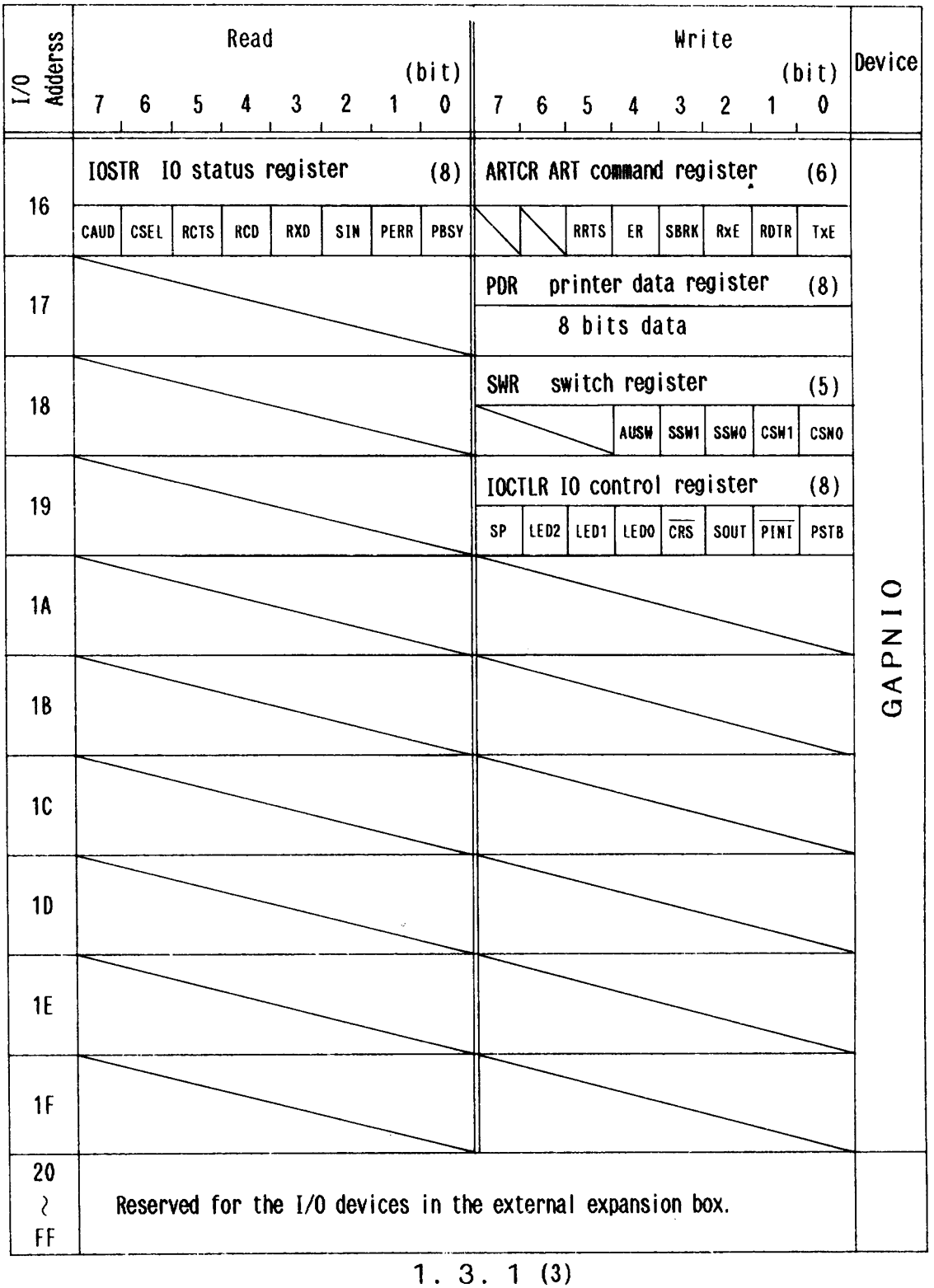
Details about the I/O registers are found in Chapter 2, "I/O Registers."

I/O Adderss	Read (bit) 7 6 5 4 3 2 1 0	Write (bit) 7 6 5 4 3 2 1 0	Device
00	ICRL・C ICR・Low command trigger (8) 8 bits data	CTLR1 control register 1 (8) BRG3 BRG2 BRG1 BRG0 SWBCR BCR1 BCR0 SLBCR	GAPNIT
01	ICRH・C ICR・High command trigger (8) 8 bits data	CMDR command register (3) RESET OVF / RESET RDYSIO / SET RDYSIO	
02	ICRL・B ICR・Low barcode trigger (8) 8 bits data	CTLR2 control register (2) RMT MIC	
03	ICRH・B ICR・High barcode trigger (8) 8 bits data		
04	ISR interrupt status register (5) EXT OVF ICF RxRDY 7508	IER interrupt enable register (5) EXT OVF ICF RxRDY 7508	
05	STR status register (8) BANK3 BANK2 BANK1 BANK0 RDYSIO RDY BCRD EAR	BANKR bank register (8) BANK3 BANK2 BANK1 BANK0 *EDU *ECA CKSW1 CKSW0	
06	SIOR serial IO register (8) 8 bits data	SIOR serial IO register (8) 8 bits data	
07			
08		VADR VRAM start address register (5) A15 A14 A13 A12 A11	GAPNDI
09		YOFF Y offset register (7) DSP Y5 Y4 Y3 Y2 Y1 Y0	
0A		FR frame register (4) F3 F2 F1 F0	

1. 3. 1 (1)


I/O Adderss
Read
(bit)
7 6 5 4 3 2 1 0
Write
(bit)
7 6 5 4 3 2 1 0
Device
0B
SPUR speed-up register (6)
PRE2 PRE1 PRE0 POST2 POST1 POST0
0C
0D
0E
0F
GAPNDL
10
11
12
13
CTG IF
(cartridge interface)
address space
CTG IF
(cartridge interface)
address space
GAPNIO
14
ARTDIR ART data input register (8)
7/8 bits data
ARTDOR ART data output register (8)
7/8 bits data
15
ARTSR ART status register (7)
RDSR FE OE PE Tx empty Rx RDY Tx RDY
ARTMR ART mode register (4)
STOP EVEN PEN DATA

1.3.1 (2)


I/O Adderss
Read
(bit)
7 6 5 4 3 2 1 0
Write
(bit)
7 6 5 4 3 2 1 0
Device
16
IOSTR IO status register (8)
CAUD CSEL RCTS RCD RXD SIN PERR PBSY
ARTCR ART command register (6)
RRTS ER SBRK RxE RDTR TxE
17
PDR printer data register (8)
8 bits data
18
SWR switch register (5)
AUSW SSW1 SSW0 CSW1 CSN0
19
IOCTLR IO control register (8)
SP LED2 LED1 LED0 CRS SOUT PINT PSTB
1A
1B
1C
1D
1E
1F
GAPNIO
20
~
FF
Reserved for the I/O devices in the external expansion box.

1. 3. 1 (3)

1.4 Miscellaneous

1.4.1 Z-80 Wait Operation

The PINE uses part of the DRAM address space as a video RAM area. Since the M1 cycle is too short to successfully access the VRAM area, the PINE Z-80 CPU inserts one wait state into every M1 cycle. This means that one wait state is inserted into every M1 cycle while an application program is being executed in DRAM. No wait state is insert when a program on ROM is executed and no DRAM is accessed. It follows from this discussion that the same program executes at different execution speeds when it is executed in DRAM and when it is implemented on ROM.

CHAPTER 2 I/O REGISTERS

CHAPTER 2 I/O REGISTERS

This chapter describes the I/O registers, their usage, and their relationship to the PINE operating system.

2.1 General

The PINE I/O registers are located in I/O port addresses P00H through PFFH. I/O addresses P00H through P1FH are for the internal I/O devices and P20H through PFFH for the external I/O devices.

The optional external RAM disk unit uses I/O addresses P90H through P94H. I/O address P94H is used in the read mode to check the presence or absence of the external RAM disk so it is not available to the user when an external device is used (through the system bus).

Since the output state of some I/O registers is maintained by the operating system, the user program must rewrite the corresponding system RAM areas when rewriting such I/O registers. (See Section 2.3, "Programming Considerations").

2.2 I/O Register Descriptions

2.2.1 P00H: ICRL.C (Input Capture Register Low Command Trigger) (read mode)

Bit	Name	Description
7	ICR 7	Input capture register lower order 8 bits
6	ICR 6	
5	ICR 5	
4	ICR 4	
3	ICR 3	
2	ICR 2	
1	ICR 1	
0	ICR 0	

Explanation:
P00H is assigned to the lower 8 bits of the input capture register. The contents (both higher and lower order bytes) of the FRC (Free Running Counter) are latched into the ICR (Input Capture Register) immediately when this register is read. The higher order value can be obtained by reading I/O address P01H (ICRHC).

P00H is used to read the contents of the FRC.

2.2.2 PØØH: CTLR1 (Control Register 1) (write mode)

Bit	Name	Description
7 6 5 4	BRG 3 BRG 2 BRG 1 BRG 0	Band Rate Generator Select
3	SWBCR	Power switch for +5vdc power to the barcode reader =1 : Power on =0 : Power off
2 1	BCR1 (up) BCR0(down)	Barcode mode select
0	SLBCR	Selects the trigger signal for latching the FRC data into the FRC. =1 : Barcode reader input =0 : External cassette ear input

Explanation:
BRG3-BRGØ specify the baud rate for the serial interface and BCR1 and BCR2 specify the polarity of the ICR trigger.

Band Rate Generator Select

B R G				Transmit		Receive	
3	2	1	0	T×C	Baud rate	R×C	Baud rate
0	0	0	0	1.74545 k	110	1.74545 k	110
0	0	0	1	2.4 k	150	2.4 k	150
0	0	1	0	4.8 k	300	4.8 k	300
0	0	1	1	9.6 k	600	9.6 k	600
0	1	0	0	19.2 k	1.2 k	19.2 k	1.2 k
0	1	0	1	38.4 k	2.4 k	38.4. k	2.4 k
0	1	1	0	76.8 k	4.8 k	76.8 k	4.8 k
0	1	1	1	153.6 k	9.6 k	153.6 k	9.6 k
1	0	0	0	19.2 k	1.2 k	1.2 k	75
1	0	0	1	1.2 k	75	19.2 k	1.2 k
1	0	1	0	307.2 k	19.2 k	307.2 k	19.2 k
1	0	1	1	614.4 k	38.4 k	614.4 k	38.4 k
1	1	0	0	3.2 k	200	3.2 k	200

Barcode mode select settings

BCR1	BCR0	Trigger polarity
0	0	Trigger inhibit
0	1	 Falling-edge trigger
0	1	 Rising-edge trigger
0	1	 Rising-/falling-edge trigger

Programming note:
The PINE OS stores the write data to the CTLR1 in system RAM area RZCTLR1 (ØFØØlH) for use during update processing.
When writing the CTLR1 directly from a user program, therefore, it is necessary to rewrite the contents of the RZCTLR1 simultaneously. The bit format of the RZCTLR1 is identical to that of the CTLR1.
Example: Turning on barcode power

```
LD   A, (RZCTLR1)
OR   Ø8H
LD   (RZCTLR1), A
OUT  (CTLR1), A
```

The OS also updates the baud rate setting through BIOS RSIOX or during accesses to the FDD.

2.2.3 PØlH: ICRH.C (Input Capture Register High Command Trigger) (read mode)

Bit	Name	Description
7	ICR 15	Input capture register higher order 8 bits
6	ICR 14	
5	ICR 13	
4	ICR 12	
3	ICR 11	
2	ICR 10	
1	ICR 9	
0	ICR 8	

Explanation:
PØlH is read to fetch the contents of the FRC. Bits ICR15-ICR8 are latched immediately when the ICRLC (PØØH) is read.
Accordingly, the ICRLC must be read before the ICRHC is read.

2.2.4 PØ1H: CMDR (Command Register) (write mode)

Bit	Name	Description
7 6 5 4 3		Ignored
2	RES OVF	=1 : Resets the INTR signal set by an FRC overflow interrupt. =0: Does nothing.
1	RES RDYSIO	=1 : Resets the RDYSIO signal (indicating the 75Ø8ready state). =0 : Does nothing.
0	SET RDYSIO	=1 : Sets the RDYSIO signal used for communication with the 75Ø8. =0 : Does nothing. This bit is used only the system.

Programming note:
The PINE OS uses the RES OVF bit during OVF interrupt processing and the RES RDYSIO bit during communication with the 75Ø8.

2.2.5 PØ2H: ICRL.B (Input Capture Register Low Barcode Trigger) (read mode)

Bit	Name	Description
7	ICR 7	Input capture register lower order 8 bits set by the state transition of the barcode or external cassette signal.
6	ICR 6	
5	ICR 5	
4	ICR 4	
3	ICR 3	
2	ICR 2	
1	ICR 1	
0	ICR 0	

Explanation:
PØ2H is assigned to the lower 8 bits of the ICR which are loaded with data from the FRC on the negative-to-positive or positive-to-negative transition of the barcode (BCRD) or external cassette (EAR) signal. The transition of the BCRD or EAR signal is identified by the INT2 signal (ICF) being made active. Either barcode reader or external cassette is selected by the CTLR1, bit SWBCR.

2.2.6 PØ2H: CTLR2 (Control Register) (write mode)

Bit	Name	Description
7		Ignored
6		
5		
4		
3		
2		
1	RMT	Turns on or off the external cassette remote mode,ready state). =1 :Turns on remote mode. =0 :Turns off remote mode.
0	MIC	Write signal (MIC output) to the external cassettedrive.

Explanation:
PØ2H is used to control the RMT and MIC lines of the external cassette interface.

Programming note:
The PINE OS does not support the external cassette. It is supported only by BASIC.

2.2.7 PØ3H: ICRH.B (Input Capture Register High Barcode Trigger) (read mode)

Bit	Name	Description
7	ICR 15	Input capture register higher order 8 bits set by the state transition of the barcode or external cassette signal.
6	ICR 14	
5	ICR 13	
4	ICR 12	
3	ICR 11	
2	ICR 10	
1	ICR 9	
0	ICR 8	

Explanation:
PØ2H is assigned to the higher 8 bits of the ICR which are loaded with data from the FRC on the negative-to-positive or positive-to-negative transition of the barcode (BCRD) or external cassette (EAR) signal. Reading this register resets the INT2 signal (ICF) that is made active by the transition of the BCRD or EAR.

2.2.8 P04H: ISR (Interrupt Status Register) (read mode)

Bit	Name	Description
7 6 5		Always set to 0.
4	INT4(EXT)	External interrupt signal. Reset by returning a response signal to the external expansion box.
3	INT3 (OVF)	Interrupt signal set when an FRC overflow condition occurs. Reset by setting the CMDR (P01H) RES OVF bit to 1.
2	INT2 (ICF)	Interrupt signal set immediately when the the FRC data is latched into the ICR on the state transition of the barcode (BCRD) or external cassette (EAR) signal. This interrupt does not occur when latching is inhibited. This bit is reset by reading ICRH.B (at P03H).
1	INT1 (ART)	Interrupt signal set when the ART RxRDY signal is set to 1. Reset by reading ARTDIR (P14H).
0	INT0 (7508)	Interrupt signal generated by the 7508 slave CPU. Reset by giving a response to the 7508.

Explanation:
INT4 through INT0 can be read even if the corresponding interrupts are masked off. INT0 is given the highest priority and INT4 the lowest priority.

Programming note:
The PINE OS uses 7508, ART, and OVF interrupts.

2.2.9 PØ4H: IER (Interrupt Enable Register) (write mode)

Bit	Name	Description
7 6 5		Ignored
4	IER 4	INT4 (EXT) interrupt status. 1 : Enable 0 : Disable
3	IER 3	INT3 (OVF) interrupt status. 1 : Enable 0 : Disable
2	IER 2	INT2 (ICF) interrupt status. 1 : Enable 0 : Disable
1	IER 1	INT1 (ART) interrupt status. 1 : Enable 0 : Disable
0	IER 0	INTØ (75Ø8) interrupt status. 1 : Enable 0 : Disable

Explanation:
The IER bits indicate the interrupt status of the corresponding interrupts.

Programming note:
The PINE OS stores the write data to the IER in system RAM area RZIER (ØF53EH) for use during update processing.
When writing the IER directly from a user program, therefore, it is necessary to rewrite the contents of the RZIER simultaneously.
The bit format of the RZIER is identical to that of the IER.

Example: Enabling EXT interrupts

```
        DI
        LD    A, (RZIER)          RZIER:(ØF53EH)
        OR    1ØH                 IER: (Ø4H)
        LD    (RZIER),A
        OUT   (IER),A
        EI
```

The PINE OS turns on and off the interrupt mask using BIOS MASKI.

In the normal state, 75Ø8 and OVF interrupts are enabled and ART interrupt is enabled when the BIOS RSIOX open function is executed and disabled when the BIOS RSIOX close function is executed. ICF and EXT interrupts are disabled.

2.2.10 P05H: STR (Status Register) (read mode)

Bit	Name	Description
7	BANK 3	Main Memory Bank Register
6	BANK 2	
5	BANK 1	
4	BANK 0	
3	RDYSIO	Controls the serial bus used to interface to the 7508 slave CPU. =1: Enables access to the 7508. =0: Disables access to the 7508.
2	RDY	RDY signal from the 7508. Normally not used.
1	BCRD	Data input from the barcode reader.
0	EAR	Data input from the external cassette.

Explanation:
See Section 1.2, "Address Map" for the values of BANK3 through BANK0.

2.2.11 P05H: BANKR (Bank Register) (write mode)

Bit	Name	Description
7	BANK 3	Main Memory Bank Register
6	BANK 2	
5	BANK 1	
4	BANK 0	
3	EDU	Development board enable signal. 1: Uses the RAM on the development board. 0: Does not use the RAM on the development board. Normally set to 0.
2	ECA	RAM select signal for the development board. Normally set to 0.
1	CKSW 1	Clock Switch
0	CKSW 0	

Explanation:
See Section 1.2, "Address Map" for the values of BANK3 through BANK0.

Programming note:
The PINE OS stores the write data to the BANKR in system RAM area RZBANKR (0F53DH) for use during update processing.
When writing the BANKR directly from a user program, therefore, it is necessary to rewrite the contents of the RZBANKR simultaneously.
The bit format of the RZBANKR is identical to that of the BANKR.

Clock Switch

CKSW1	CKSW0	System clock
1	0	3.6864 MHZ
1	1	3.072 MHZ
0	*	3.4576 MHZ

* : Ignored

Note: For the PINE, CKSW1 must be set to 1 and CKSWØ to Ø because the PINE uses the 3.6864 MHz system clock. Setting these bits to other values may cause serial I/F or timer malfunctions.

The PINE OS provides LOADX, STORX, LDIRX, JUMPX, and CALLX as BIOS functions for controlling the banks. For details of these routines, see 4.4, "Bank Switching" in Part II.

2.2.12 PØ6H: SIOR (Serial I/O Register) (read/write mode)

Bit	Name	Description
7	SIO 7	7508 data register
6	SIO 6	
5	SIO 5	
4	SIO 4	
3	SIO 3	
2	SIO 2	
1	SIO 1	
0	SIO 0	

Explanation:
PØ6H holds 8-bit data received from the 75Ø8 in the read mode and 8-bit data to be sent to the 75Ø8 in the write mode.

2.2.13 PØ8H: VADR (VRAM Start Address Register) (write mode)

Bit	Name	Description
7	A15	V-RAM Start Address
6	A14	
5	A13	
4	A12	
3	A11	
2		Ignored
1		
0		

Explanation:
The VADR addresses the VRAM area. It generates the five highest order address bits, providing a VRAM address space of (A15 A14 A13 A12 A11 Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø) to (A15 A14 A13 A12 A11 1 1 1 1 1 1 1 1 1 1). This allows the VRAM area to be located on any 2K-byte boundary.

Programming note:
The PINE OS allocates addresses ØD8ØØH through ØDFFFH for the system screen VRAM (VRAM2) and addresses ØEØØØH through ØE7FFH for the user screen VRAM (VRAM1).

The address of the currently active VRAM is stored in LSCRVRAM (ØF294H). The VADR is loaded with the address data from LSCRVRAM + 1 (F295H).

2.2.14 PØ9H: YOFF (Y Offset Register) (write mode)

Bit	Name	Description
7	DSP	Turns on and off LCD display. =1: Turns on display. =0: Turns off display.
6		Ignored
5	Y5	Y-direction offset register (YOFF)
4	Y4	
3	Y3	
2	Y2	
1	Y1	
0	Y0	

Explanation:
The YOFF defines the correspondence between the VRAM and the LCD panel. It gives the offset with respect to the top of the VRAM at which display is to start. When display reaches the bottom of the VRAM, it wraps around to the top of the VRAM. One screenful of display ends at (YOFF - 1)th dot line.

Programming note:
The PINE OS uses the YOFF for vertical scrolling. The current value of the YOFF is saved in LVRAMYOFF (ØF2AØH).

2.2.15 PØAH: FR (Frame Register) (write mode)

Bit	Name	Description
7		Ignored
6		
5		
4		
3	FR3	Frame Register
2	FR2	
1	FR1	
0	FR0	

Explanation:
The FR defines the LCD frame frequency. The table below shows the relationship between the frame register and frame frequencies.

FR				LCD frame frequency (in Hz)		
FR3	FR2	FR1	FR0	3.68MHz	3.07MHz	2.45MHz
0	1	0	0	106	88	70
0	1	0	1	86	72	57
0	1	1	0	72	60	48
0	1	1	1	62	52	41
1	0	0	0	55	46	36
1	0	0	1	49	41	32
1	0	1	0	44	37	29
1	0	1	1	40	33	Invalid
1	1	0	0	37	Invalid	Invalid
1	1	0	1	34	Invalid	Invalid

FR values (0000) through (0011), (1110), and (1111) are invalid.

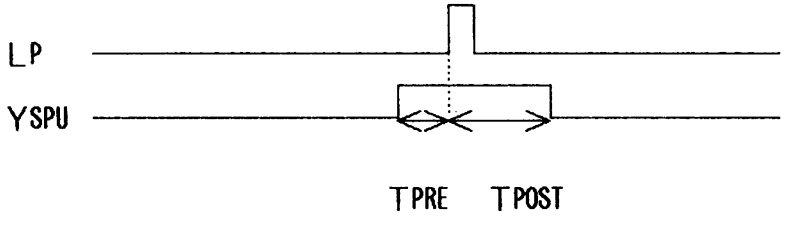
Programming note:
The 3.68 MHz column in the table applies to the PINE since its system clock is 3.6864 MHz. The PINE OS loads the FR with Ø6H when executing the power-on, reset, and system initialize functions.

2.2.16 PØBH: SPUR (SpeedUp Register) (write mode)

Bit	Name	Description
7		Ignored
6	PRE2	Define TPRE.
5	PRE1	
4	PRE0	
3		Ignored
2	POST2	Define TPOST.
1	POST1	
0	POST0	

Explanation:
The SPUR defines the timing at which the impedance of the power supply to the LCD is to be reduced to suppress the voltage fluctuations occurring (due to increased current) during the rewrite of LCD panel data.

TPRE and TPOST define the pulse width of the YSPU which is used to save the power to the LCD unit. TPRE specifies the time interval before the LP signal and TPOST the delay time after LP. LP an LCD control signal and gives the latch pulse to the LCD shift register.



The table below lists the TPRE and TPOST values for the frame frequency of 50. The actual time values can be obtained from:

$$\text{TPRE (TPOST)} = \frac{50}{\text{Frame frequency}} \times \text{(Value taken from table)}$$

PRE2	PRE1	PRE0	TPRE (μs)
0	0	0	77
0	0	1	67
0	1	0	57
0	1	1	48
1	0	0	38
1	0	1	28
1	1	0	18
1	1	1	9.2

POST2	POST1	POST0	T POST (μs)
0	0	0	0.2
0	0	1	9.9
0	1	0	19
0	1	1	29
1	0	0	39
1	0	1	48
1	1	0	58
1	1	1	68

Programming note:
The PINE OS loads the SPUR with 43H when executing the power-on, reset, and system initialize functions.

2.2.17 P1ØH - P13H

Explanation
P1ØH through P13H are reserved for the cartridge interface. Their assignments differ depending on the cartridge mode (HS, DB, IO, or OT mode). See Section 4.1, "Cartridge Interface" for details about P1ØH through P13H.

2.2.18 P14H: ARTDIR (ART Data Input Register) (read mode)

Bit	Name	Description
7	RD7	Receive data.
6	RD6	
5	RD5	
4	RD4	
3	RD3	
2	RD2	
1	RD1	
0	RD0	

Explanation:
P14H is loaded with the parallel data converted from the serial data received over the RxD line. Bit 7 (RD7) is set to Ø when the 7-bit data format is used.

Programming note:
In PINE OS, serial data reception is conducted by an interrupt processing routine and the transfer of received data to the application program is done by a BIOS RSIOX function.

2.2.19 P14H: ARTDOR (ART Data Output Register) (write mode)

Bit	Name	Description
7	TD7	Send data.
6	TD6	
5	TD5	
4	TD4	
3	TD3	
2	TD2	
1	TD1	
0	TD0	

Explanation:
P14H is loaded with the parallel data to be sent over the serial TxD line. Bit 7 (TD7) is ignored when the 7-bit data format is used.

Programming note:
In PINE OS, serial data transmission and interface to the application program are conducted by BIOS RSIOX functions.

2.2.2Ø P15H: ARTSR (ART Status Register) (read mode)

Bit	Name	Description
7	RDSR	Data Set Ready signal. Set to 1 when the RS-232C interface DSR terminal is set active.
6		Always set to Ø.
5	FE	Set to 1 to indicate a framing error.
4	OE	Set to 1 to indicate an overrun error.
3	PE	Set to 1 to indicate a parity error.
2	Tx Empty	Indicates that no data is present in the transmitter block. This bit is set when the ARTDOR transmit buffer and the parallel-to-serial converter are both empty.
1	Rx RDY	When set to 1, generates an INT1 (ART) interrupt request to the Z-8Ø CPU to indicate that a data byte is received from the serial communication line. RxRDY is reset by reading the ARTDIR receive buffer (P14H). This bit may also be reset by the reset input or error reset command.
0	Tx RDY	Set to 1 when the ARTDOR output buffer is emptied and reset when the buffer is loaded with send data.

Explanation:

FE (bit 5): The receive data processing is not affected when a framing error condition occurs. The PINE continues to receive the next data byte and checks it against the framing error condition. If the stop bits are received normally, the PINE resets the FE bit.

OE (bit 4): The receive data processing continues even when an overrun error occurs. The OE, however, is not reset when the next data byte is received normally. The OE bit can be reset only by issuing the error reset command (ER = 1) or reset signal.

PE (bit 3): The resetting conditions for the PE bit are identical to those for the FE bit. Parity is checked only when PEN is set to 1, that is, PE is held at Ø when PEN is Ø.

2.2.21 P15H: ARTMR (ART Mode Register) (write mode)

Bit	Name	Description
7	STOP	Specifies the number of stop bits. =1 : 2bit =0 : 1bit
6		Ignored
5	EVEN	Specifies the parity check mode (valid only when PEN is 1). =1 : Even parity =0 : Odd parity
4	PEN	Enables or disables parity checking. =1 : Enables parity checking. =0 : Disables parity checking.
3		Ignored
2	DATA	Specifies the length of the serial data. =1 : 8bit =0 : 7bit
1 0		Ignored

Programming note:
The PINE OS stores the ARTMR data in RZARTMR (ØFØØ3H) in the system RAM area for use during update processing. When writing the ARTMR directly from a user program, therefore, it is necessary to rewrite the contents of the RZARTMR simultaneously. The bit format of the RZARTMR is identical to that of the ARTMR.

Writing data to the ARTMR is supported by a BIOS RSIOX function.

2.2.22 P16H: IOSTR (IO Status Register) (read mode)

Bit	Name	Description
7	CAUD	Audio input signal from the cartridge connector (has nothing to do with AUSW).
6	CSEL	Cartridge option select signal. =0 : HS (Hand Shake) mode =1 : Other modes
5	RCTS	RS-232C CTS signal. Set to 1 when RS-232C CTS is set active.
4	RCD	RS-232C CD signal. Set to 1 when RS-232C CD is set active.
3	RXD	Serial data input.
2	SIN	Status signal from the SIO interface.
1	PERR	Error signal from the Centronics interface (A 1 in this bit indicates a printer error condition).
0	PBUSY	Busy signal from the Centronics interface (A 1 in this bit indicates a printer busy condition).

Explanation:
The state of the ART inputs (RDSR, RCTS, RCD, etc.) is determined as follows:

2.6 volts and up:	High (active)
0.7 to 2.6 volts:	Unpredictable
0.7 volts and below:	Low (inactive)

2.2.23 P16H: ARTCR (ART Command Register) (write mode)

Bit	Name	Description
7 6		} Ignored
5	RRTS	RS-232C RTS signal. Setting the RRTS bit to 1 sets the RTS pin in the RS-232C interface active.
4	ER	Resets the OE, FE, and PE bits. ER must be set to 1 when RXE is set to 1. Setting ER to 1 generates a pulse (only during the write operation) so it need not be reset.
3	SBRK	Break output. Setting this bit to 1 forces the TXD line to Ø (valid only when TXE is 1).
2	RXE	Enables or disables serial reception. =1 : Enable =0 : Disable
1	RDTR	RS-232C DTR signal. Setting this bit to 1 sets the DTR pin in the RS-232C interface active.
0	TXE	Enables or disables serial transmission. =1 : Enable =0 : Disable TXD is held in the 1 (mark) level while TXE is Ø.

Programming note:
The PINE OS stores the ARTCR data in RZARTCR (ØFØØ4H) in the system RAM area for use during update processing. When writing the ARTCR directly from a user program, therefore, it is necessary to rewrite the contents of the RZARTCR simultaneously. The bit format of the RZARTCR is identical to that of the ARTCR.

Writing data to the ARTCR is supported by a BIOS RSIOX function.

2.2.24 P17H: PDR (Printer Data Register) (write mode)

Bit	Name	Description
7	PDR7	Print data to the Centronics interface
6	PDR6	
5	PDR5	
4	PDR4	
3	PDR3	
2	PDR2	
1	PDR1	
0	PDR0	

Explanation:
See Section 4.4, "Other Interfaces" for the method of transferring print data to the Centronics interface.

Programming note:
Writing data to the Centronics interface is supported by the BIOS LIST function.

2.2.25 P18H: SWR (Switch Register) (write mode)

Bit	Name	Description
7		Ignored
6		
5		
4	AUSW	Used to mask on or off the CAUD input from the cartridge. =0 : Masks off CAUD. =1 : Masks on CAUD.
3	SSW1	Serial mode
2	SSW0	
1	CSW1	Cartridge I/F mode
0	CSW0	

Explanation:
P18H is used to define the mode of the serial and cartridge interfaces.

Serial mode

SSW1	SSW0	RXD	TXD
0	0	Cartridge SIO	Cartridge SIO
0	1	SIO	SIO
1	0	RS-232C	RS-232C
1	1	RS-232C	SIO

Cartridge mode

CSW1	CSW0	Mode
0	0	HS (HandShake mode)
0	1	IO (Input/Output) mode
1	0	DB (Data Bus) mode
1	1	OT (Output port) mode

Programming note:
The PINE OS stores the SWR data in RZSWR (ØFØØ5H) in the system RAM area for use during update processing. When writing the SWR directly from a user program, therefore, it is necessary to rewrite the contents of the RZSWR simultaneously. The bit format of the RZSWR is identical to that of the SWR.

Example: Switching the cartridge mode to the IO mode

```
          LD   A, (RZSWR)          RZSWR: (ØFØØ5H)
          AND  ØFCH                SWR: (18H)
          OR   Ø1H
          LD   (RZSWR),A
          OUT  (SWR), A
```

Switching the serial mode can be accomplished using a BIOS RSIOX function.

2.2.26 P19H: IOCTLR (IO Control Register) (write mode)

Bit	Name	Description
7	SP	Output to the loudspeaker. SP must be set to Ø when the CAUD output is to be directed to the loudspeaker. Set AUSW to Ø when directing the SP output to the loudspeaker.
6	LED2	LED output port
5	LED1	
4	LED0	
3	$\overline{CRS}$	Cartridge reset signal used to software through reset the cartridge. Setting this bit to Ø resets the cartridge.
2	$\overline{SOUT}$	Control signal to the SIO interface.
1	$\overline{PINT}$	Initial output to the Centronics interface. Setting this bit to Ø initializes the printer.
0	PSTB	Strobe signal to the Centronics interface. =0 : Normal =1 : Data strobe

Programming note:
The PINE OS stores the IOCTLR data in RZIOCTLR (ØF006H) in the system RAM area for use during update processing. When writing the IOCTLR directly from a user program, therefore, it is necessary to rewrite the contents of the RZIOCTLR simultaneously. The bit format of the RZIOCTLR is identical to that of the IOCTLR.

In the PINE OS, SP is referenced by the BIOS BEEP function and LED2 through LEDØ by the BIOS input functions. LED2 through LEDØ is controlled by the CONOUT function (ESC + (AØH to A5H)).

2.2.27 P20H-PFFH (read/write mode)

P20H through PFFH are used for external RAM disk drives and other optional units.

Although I/O addresses P20H through PFFH are always available if the system bus is used, the PINE OS examines I/O address P94H to determine whether an external RAM disk unit is connected to the system bus. This address is reserved only for the external RAM disk unit. Under the PINE OS, a 1 in bit 7 of P94H indicates that an external RAM disk unit is attached.

2.3 Programming Considerations

2.3.1 Initial I/O Register Reset

To save gate count, the outputs of some control registers in the PINE gate array LSIs are set to Ø by a special means immediately after a initial reset.
When an initial reset occurs, the outputs of control registers are masked to the Ø level by the register output control flip-flop (see Figure 2.3.1) even if their contents are unpredictable. After the CPU is started, the initial program initializes the registers and remove the register mask. Externally, the registers are given the appearance of being reset. This resetting method is called pseudo-reset.

The PINE registers are divided into three groups according to the way they are initialized:

1) Registers that are reset in the pseudo-reset mode.
2) Registers that are reset in the normal mode.
3) Registers that are not reset at all.

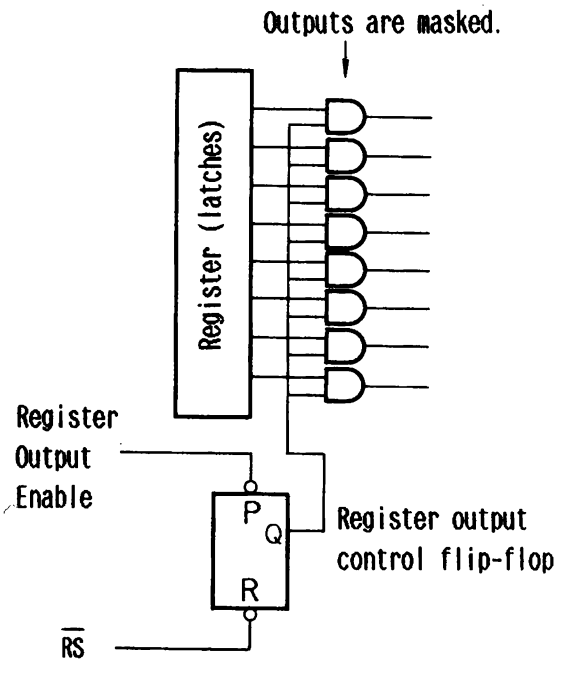


Fig. 2.3.1 Resetting a Register in Pseudo-reset mode

2.3.1.1 Registers that are reset in pseudo-reset mode

	7	6	5	4	3	2	1	0
CTLR1 (P00H)					SWBCR	BCR1	BCR0	
IER (P04H)				EXT	OVF	ICF	RxRDY	7508
BANKR (P05H)	BANK3	BANK2	BANK1	BANK0				

Registers CTLR1 (PØØH), IER (PØ4H), and BANKR (PØ5H) are reset in the pseudo-reset mode by a single output control flip-flop. Their masks are removed by writing the CTLR1 register (PØØH).

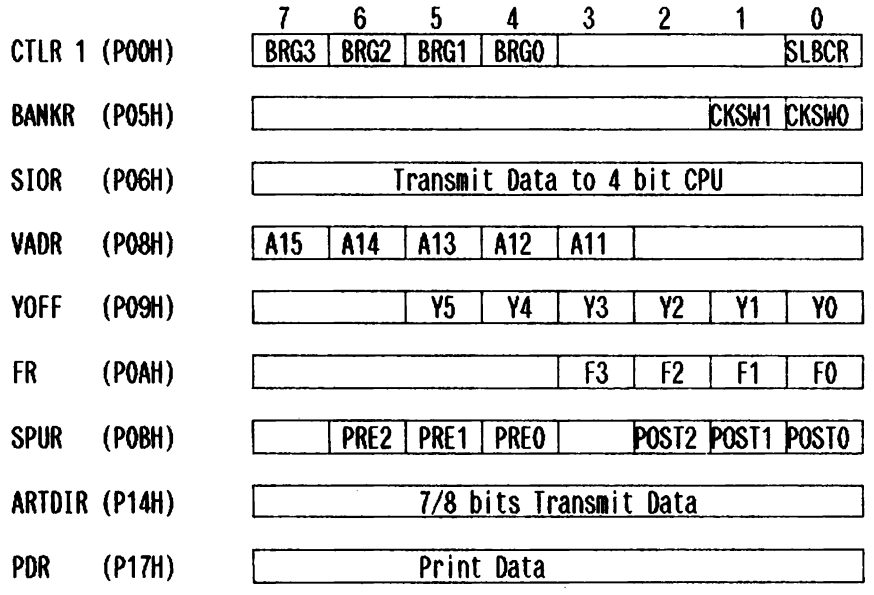
	7	6	5	4	3	2	1	0
ARTMR (P15H)	STOP		EVEN	PEN		DATA		
ARTCR (P16H)			RRTS	ER	SBRK	RXE	RDTR	TXE
SWR (P18H)				AUSW	SSW1	SSW0	CSW1	CSW0
IOCTLR(P19H)	SP	LED2	LED1	LED0	CRS	SOUT	PINT	PSTB

Registers ARTMR (P15H), ARTCR (P16H), SWR (P18H), and IOCTLR (P19H) are reset in the pseudo-reset mode by a single output control flip-flop. Their masks are removed by writing the ARTMR register (P15H).

2.3.1.2 Registers that are reset in normal mode

	7	6	5	4	3	2	1	0
CTLR2 (P02H)							RMT	MIC
YOFF (P09H)	DSP							

2.3.1.3 Registers that are not reset



2.3.2 Writing to an I/O Port

The PINE OS stores the current output state of the I/O registers in the system RAM areas. The purpose of this is to allow the user to update portions of the I/O registers and to restore the I/O register data after power shut-off. When writing these registers directly from a user program, therefore, it is necessary to rewrite the contents of the corresponding system RAM areas simultaneously. The table below lists the I/O registers and the corresponding system RAM areas.

I/O Address	Name	RAM Address	Variable Name	Remarks
P00H	CTLR1	F001H	RZCTLR1	
P04H	IER	F53EH	RZIER	Must be set to DI state during update.
P05H	BANKR	F53DH	RZBANKR	Another procedure is required when actually switching banks.
P15H	ARTMR	F003H	RZARTMR	
P16H	ARTCR	F004H	RZARTCR	
P18H	SWR	F005H	RZSWR	
P19H	IOCTLR	F006H	RZIOCTLR	

CHAPTER 3 7508 CPU

CHAPTER 3 7508 CPU

This chapter describes the 7508 slave CPU commands and functions and how to transfer data to and from the 7508.

See Sections 3.5, "Keyboard" and 4.7, "Interrupts" in Part II, "Software" for details.

3.1 7508 CPU Functions

The 7508 CPU performs the following functions:
(1) Controlling keyboard functions such as keyboard scan.
(2) Turning on and off the main CPU switch.
(3) Controlling the RESET button.
(4) Monitoring the battery voltage and switching batteries.
(5) Performing the alarm function.
(6) Performing the 1-second interval timer function.
(7) Controlling the power switch.
(8) Controlling the calendar and clock.
(9) Controlling DRAM refreshing.
(10) Transferring serial data to and from the main CPU.

In addition to generating interrupts, the 7508 CPU transfers commands and data to and from the Z-80 CPU via a serial data line using a handshaking technique.

The processing results for functions (1) through (7) above are returned to the Z-80 in the form of interrupts. The Z-80 identifies the interrupt source by reading the 7508 status code.

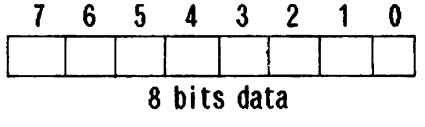
3.2 Interfaces

3.2.1 I/O Ports

The PINE Z-80 CPU uses the following I/O ports when transferring data or commands to and from the 7508 CPU:

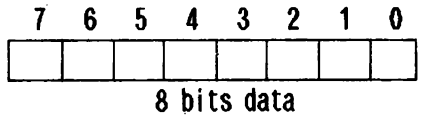
(1) Serial data communication

P06H Read (SIOR)



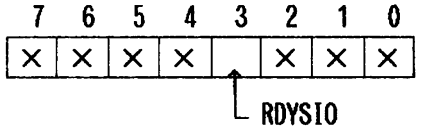
Data from the 7508

P06H Write (SIOR)



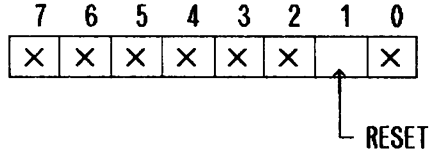
Commands or data to be sent to the 7508

P05H Read (STR)



RDYSIO = 0 : Access inhibited
= 1 : Access allowed

P01H Write (CMDR)

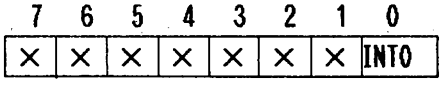


Used to control the RDYSIO control signal.

Reset RDYSIO = 0 : Does nothing.
= 1 : Resets.

(2) Interrupt handling

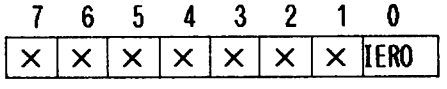
P04H Read (ISR)



Used to inform the Z-80 CPU that an interrupt occurred in the 7508.

INT0 = 0 : No interrupt has occurred.
= 1 : An interrupt has occurred.

P04H Write (IER)



Used to disable the 7508 for interrupts.

IER0 = 0 : Disabled
1 : Enabled

Bits marked with X are not affected by the 7508 CPU.

3.2.2 Transferring Data and Commands to and from the 7508 CPU

This subsection describes the procedures for transferring commands or data to and from the 7508 CPU.

(1) Sending commands or data to the 7508

The flowchart in Figure 3.2.1 illustrates the procedure for sending commands or data to the 7508.

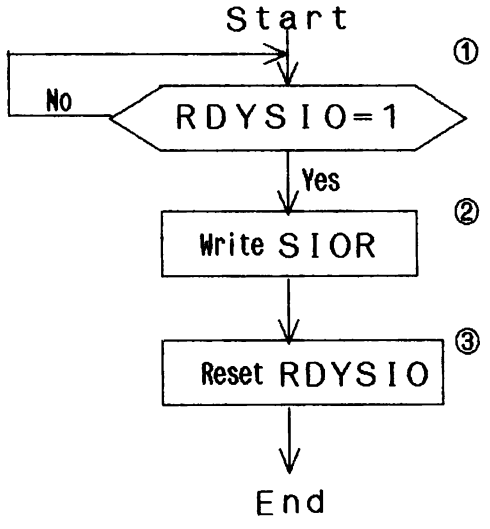


Figure 3.2.1 Procedure for Sending a Command or Data

When one or more data bytes are to be sent following the command, the above procedure is repeated the number of times equal to the number of the commands and data bytes.

Step	Processing	Description
1	RDYSIO = 1 ?	* Read P05H and check whether or not the 7508 is ready to receive a command or data byte. * If bit 3 = 1, go to step 2. If bit 3 = 0, repeat step 1.
2	Write SIOR	* Write a command or data byte into P06H to send it to the 7508.
3	Reset RDYSIO	* Reset the 7508 RDYSIO signal and write 02H into P01H.

(2) Receiving data from the 7508

The flowchart in Figure 3.2.2 illustrates the procedure for receiving data from the 7508 CPU.

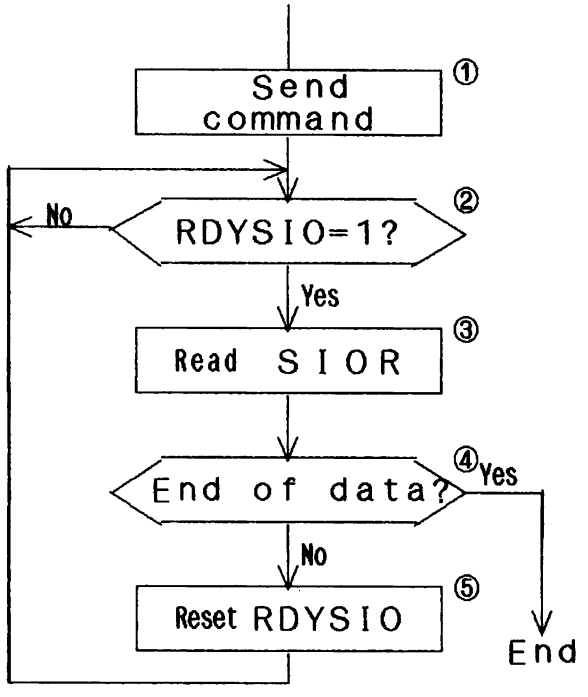


Figure 3.2.2 Procedure for Receiving Data

Step	Processing	Description
1	Send command	* Send a command according to the flowchart in Figure 3.2.1.
2	RDYSIO = 1 ?	* Read P05H and check whether or not the main CPU is ready to receive data from the 7508 CPU. If bit 3 = 1, go to step 3. If bit 3 = 0, repeat step 2.
3	Read SIOR	* Read P06H to get data from the 7508.
4	End of data?	* Check whether or not the main CPU received the number of data bytes specified in the command. Go to step 5 if there is any more data to be received.
5	Reset RDYSIO	* Reset the 7508 RDYSIO signal and write 02H into P01H.

3.2.3 Points to Remember When Using the 7508

The following points should be noted when transferring commands or data directly to and from the 7508 CPU:

(1) Remember to disable 7508 interrupts when transferring commands or data to or from the 7508 CPU.
Interrupts can be disabled by:
- DI instruction.
- Rewriting the IER (P04H).
- BIOS MASKI function.

The 7508 must be disabled for interrupts while the procedures shown in figures 3.2.1 and 3.2.2. are being executed.

(2) Complete the send or receive sequence for a command before proceeding with the next command. Normal processing cannot be guaranteed unless the application program sends or receives the required number of data bytes.

3.3 7508 Commands

This section gives a detailed description of 7508 commands. See Section 3.2 for the procedure for transferring data or commands to and from the 7508.

The table below lists the commands that the 7508 CPU accepts from the main CPU.

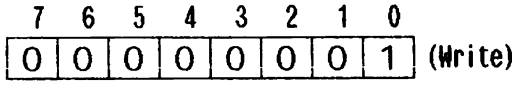
No.	Command function	Code	No.	Command function	Code
1	Power OFF	01H	14	Power Switch Read	08H
2	Read Status	02H	15	Alarm Read	09H
3	KB Reset	03H	16	Alarm Set	19H
4	KB Repeat Timer 1 Set	04H	17	Alarm OFF	29H
5	KB Repeat Timer 2 Set	14H	18	Alarm ON	39H
6	KB Repeat Timer 1 Read	24H	19	DIP Switch Read	0AH
7	KB Repeat Timer 2 Read	34H	20	Stop Key Interrupt disable	0BH
8	KB Repeat OFF	05H	21	Stop Key Interrupt enable	1BH
9	KB Repeat ON	15H	22	7 chr. Buffer	0CH
10	KB Interrupt OFF	06H	23	1 chr. Buffer	1CH
11	KB Interrupt ON	16H	24	1 sec. Interrupu OFF	0DH
12	Clock Read	07H	25	1 sec. Interrupt ON	1DH
13	Clock Write	17H	26	KB Clear	0EH
			27	System Reset	0FH

Commands are identified by a 1 in it bit position 7 of the command code and data by a 0 in bit position 7.

(1) Power off

Function: Turns off power to the main CPU (Z-80).

Sequence:



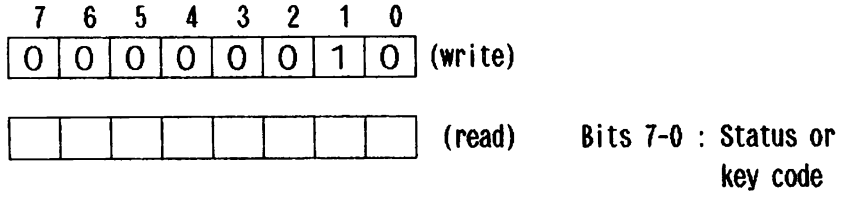
Explanation:
This command is used to turn off power to the main CPU (Z-80).

Note: This command is not available to application programs. Use the BIOS POWEROFF function in application programs.

(2) Read status

Function: Reads the 7508 status or key code.

Sequence:



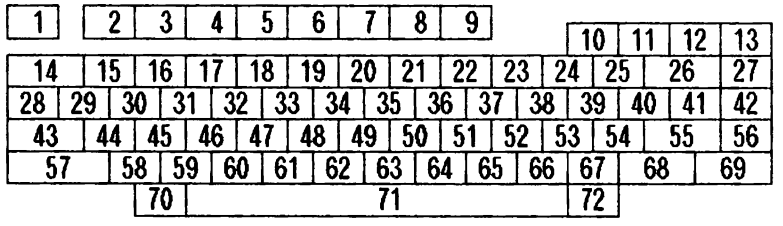
Explanation:
1) This command is used to read the 7508 status to identify the interrupt source when an interrupt occurs or after the reset state is released.
2) The status byte is classified into two types, the key code and status. The meanings of key code and status are described below.

1. Key code
Status bytes 0BEH and below indicate key code. The correspondence between the keys and key codes is shown in figures 3.3.1 and 3.3.2.

There are two types of keys, ordinary and switch keys. When an ordinary key is pressed, the 7508 returns only a make code corresponding to the key. For a switch key, however, the 7508 returns a make code (0B2H - 0B7H) when the key is pressed and a break code (0A2H - 0A7H) when it is released.

(i) Hard code table (standard keyboard)

The figure and table below show the correspondence between the keys on the standard keyboard and the key codes. Break and Make in the table indicate that the code is returned at the time the SHIFT key is pressed and released, respectively.

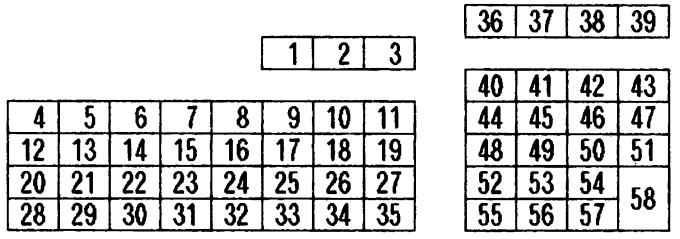


Higher / Lower	0	1	2	3	4	5	6	7	8	9	A	B
0	2	1	29	46	62	21	37	54	12			
1	3	14	30	47	63	22	38	55	13			
2	4	15	31	48	64	23	39	56			43 Break	43 Make
3	5	16	32	49	65	24	40	71			57 Break	57 Make
4	6	17	33	50	66	25	41	58			70 Break	70 Make
5	7	18	34	51	67	26	42	59			72 Break	72 Make
6	8	19	35	52	10	27	44	60			68 Break	68 Make
7	9	20	36	53	11	28	45	61			69 Break	69 Make

Figure 3.3.1 Correspondence between Key Numbers and Key Codes (Standard Keyboard)

(ii) Hard code table (item keyboard)

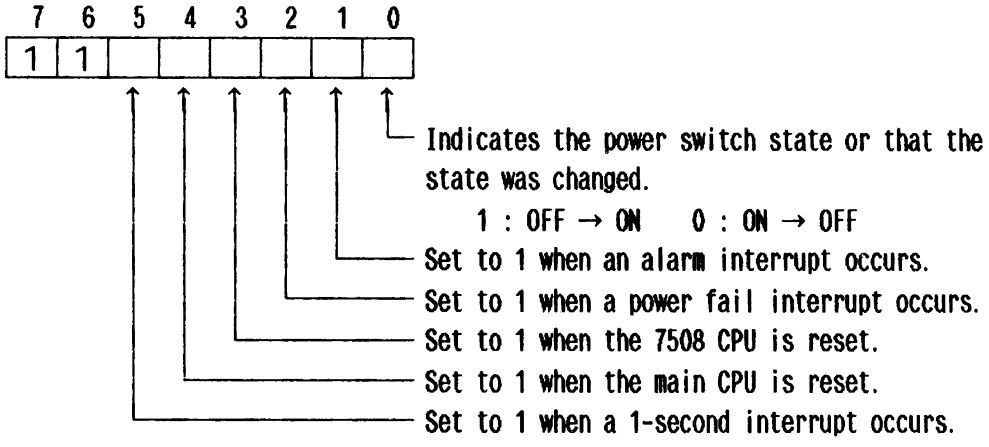
The figure and table below show the correspondence between keys on the item keyboard and key codes. Break and Make in the table indicate that the code is returned at the time the SHIFT key is pressed and released, respectively.



Higher / Lower	0	1	2	3	4	5	6	7	8	9	A	B
0			43	51	4	20	12	28				
1		36	44	52	5	21	13	29				
2		37	45	53	6	22	14	30			1 Break	1 Make
3		38	46	54	7	23	15	31				
4		39	47	55	8	24	16	32				
5		40	48	56	9	25	17	33			2 Break	2 Make
6		41	49	57	10	26	18	34			3 Break	3 Make
7		42	50	58	11	27	19				35 Break	35 Make

Figure 3.3.2 Correspondence between Key Numbers and Key Codes (Item Keyboard)

2. Status
Status bytes ØC0H and above indicate that an interrupt occurred or that the reset state was released. Otherwise, the status byte ØBFH is returned. Each bit of the status byte has the meaning listed below. When two or more interrupts or resets occur simultaneously, the corresponding bits are set to 1.

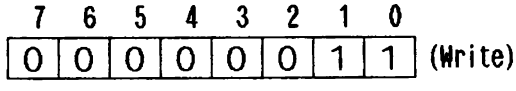


PINE OS reads this 75Ø8 status information during interrupt processing following an interrupt, or in address Ø start processing (system initialize, reset, power-on, and alarm/wake processing) when the 75Ø8 or main CPU is reset. PINE OS determines what to do next on the basis of this information.

(3) KB reset

Function: Initializes the keyboard.

Sequence:



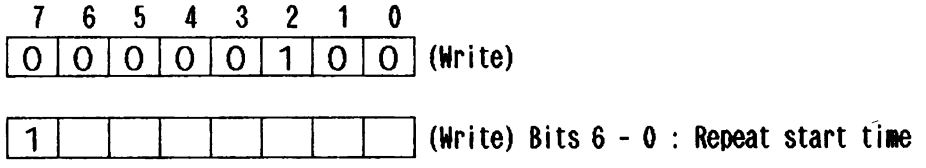
Explanation:
1) Initializes the keyboard as follows:
   - Sets the keyboard repeat start time to 656 ms.
   - Sets the keyboard repeat interval to 7Ø ms.
   - Clears the key buffer.
   - Enables interrupts from the keyboard.
2) Scans the keyboard and loads information concerning the currently pressed key into the buffer.

Note: PINE OS uses this command to initialize and reset the system.

(4) KB repeat timer 1 set

Function: Sets the keyboard repeat start time.

Sequence:



Explanation:

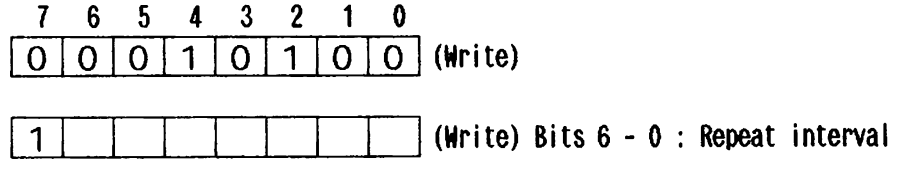
1) The corresponding key code is read repeatedly as long as an ordinary key (i.e. a key other than the switch and special keys) is held down. This command defines the interval between the time when a key is first pressed and the time when the auto repeat function starts.
2) The send data specifies the repeat start time in 1/64 second (approximately 15 ms) increments. The maximum repeat start time is approximately 2 seconds. The MSB of the data must be always set to 1.
3) The initial value is 656 ms.

Note: In PINE OS, BIOS CONOUT (ESC + ØF1H) is used to set the repeat start time.

(5) KB repeat timer 2 set

Function: Defines the keyboard repeat interval.

Sequence:



Explanation:

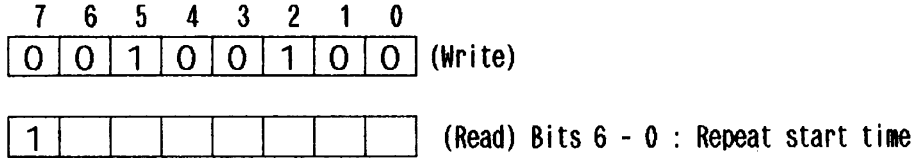
1) Defines the interval at which the key code of a key being held down is to be repeatedly entered.
2) The send data specifies the keyboard repeat interval in 1/256 second (approximately 3.9 ms) increments. The maximum period is Ø.5 second. The MSB of the data must be always set to 1.
3) The initial value is approximately 7Ø ms.

Note: In PINE OS, BIOS CONOUT (ESC + ØF2H) is used to set the repeat interval.

(6) KB repeat timer 1 read

Function: Reads the keyboard repeat start time.

Sequence:



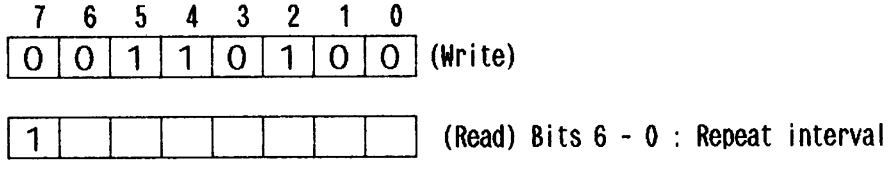
Explanation:

1) Returns the keyboard repeat start time which is currently set.
2) The receive data specifies the keyboard repeat start time in 1/64 second (approximately 15 ms) increments. The MSB of the data is always set to 1, but the repeat start time is treated as if the MSB were Ø.

(7) KB repeat timer 2 read

Function: Reads the keyboard repeat interval.

Sequence:



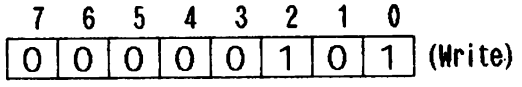
Explanation:

1) Returns the keyboard repeat interval which is currently set.
2) The receive data specifies the keyboard repeat interval in 1/256 second (approximately 3.9 ms) increments. The MSB of the data is always set to 1, but the repeat interval is treated as if the MSB were Ø.

(8) KB repeat off

Function: Disables the keyboard auto repeat function.

Sequence:



Explanation:

This command is used to disable the keyboard auto repeat function. After this command is executed, the key code is returned only once, even if the key is held down.

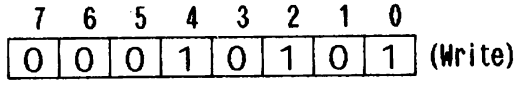
Notes:

1. In PINE OS, the KB repeat function is enabled by default when an item keyboard is installed.
2. In PINE OS, BIOS CONOUT (ESC + ØFØH) is used to switch on or off the keyboard repeat function.

(9) KB repeat on

Function: Enables the keyboard auto repeat function.

Sequence:



Explanation:

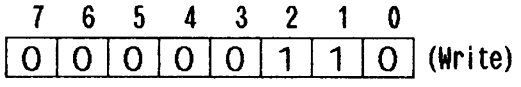
1) This command is used to enable the keyboard auto repeat function. After this command is executed, the key code is returned at every repeat interval time if a key is held down for longer than the repeat start time. The auto repeat function is invalid for switch and special keys.
2) The KB repeat function is enabled by default.

Note: In PINE OS, BIOS CONOUT (ESC + ØFØH) is used to switch the keyboard auto repeat function ON/OFF.

(10) KB interrupt off

Function: Disables the Z-80 CPU for all keyboard interrupts.

Sequence:



Explanation:

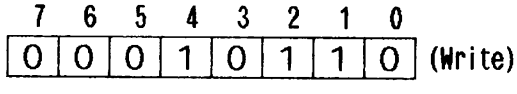
1) This command is used to disable the Z-80 CPU for keyboard interrupts. When a key is pressed after this command is executed, the key code is placed in the 7508 buffer but no interrupt request is sent to the Z-80 CPU. If command (11) is subsequently executed, any keyboard interrupt code stored in the buffer is sent to the Z-80.
2) Extra key codes are ignored when the key buffer is full. However, the STOP key code can be added to the end of the buffer.

Note: In PINE OS, this function is supported by BIOS MASKI.

(11) KB interrupt on

Function: Enables the Z-80 CPU for keyboard interrupts.

Sequence:



Explanation:

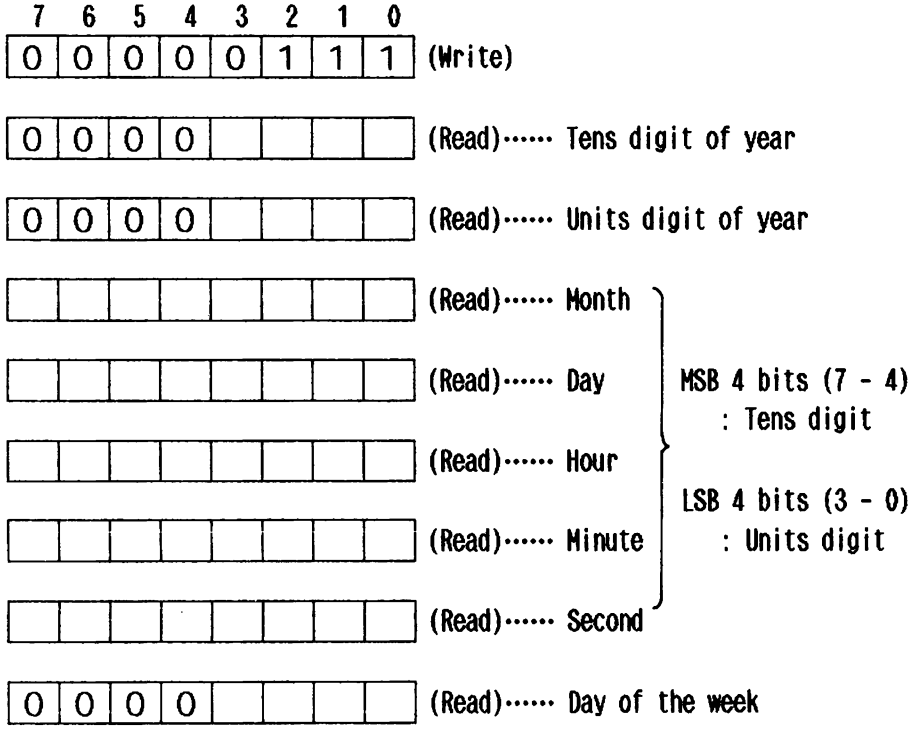
1) This command is used to enable the Z-80 CPU for keyboard interrupts.
2) KB interrupts are enabled by default.

Note: In PINE OS, this function is supported by BIOS MASKI.

(12) Clock read

Function: Reads the current time of the 7508 calendar/clock.

Sequence:



Explanation:

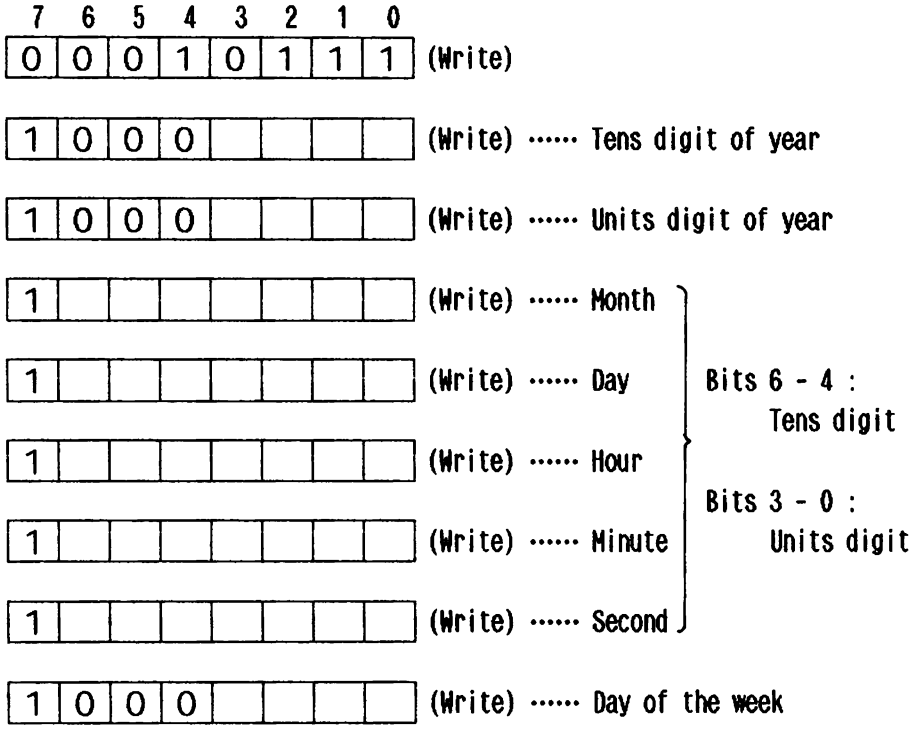
1) This command is used to read the contents of the 7508 calendar/clock.
2) The read data includes the year, month, day, hour, minute, second and day of the week. All these items are specified in BCD notation.
3) The time is expressed in the 24-hour system, and for the day of the week 0 through 6 correspond to Sunday through Saturday. Since the 7508 CPU does not check the read data, the contents of the calendar/clock cannot be guaranteed if logically invalid data was entered at the time of the last clock write.

Note: In PINE OS, this function is supported by BIOS TIMDAT.

(13) Clock write

Function: Sets the 7508 calendar/clock.

Sequence:



Explanation:

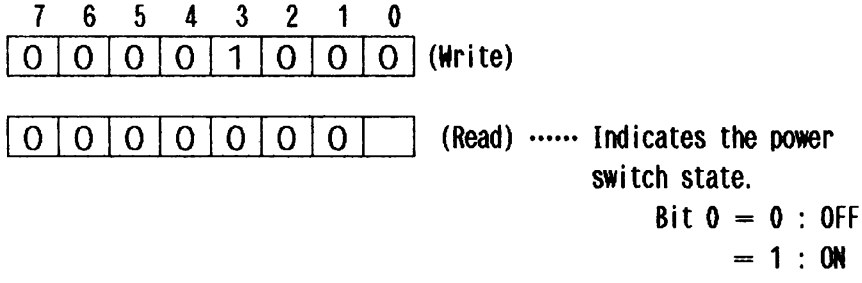
1) This command is used to specify the year, month, day, hour, minute, second and day of the week for the 7508 calendar/clock. All these items are defined in BCD notation. The MSB of send data bytes must always be set to 1.
2) The time is expressed in the 24-hour system. The day of the week is automatically updated within the range 0 through 6. Since the 7508 CPU does not check the set data, the contents of the calendar/clock cannot be guaranteed if logically invalid data is entered.
3) When partially updating the calendar/clock, set every bit of the data bytes not to be updated to 1 and send all data bytes. Items coded as 11111111 will be ignored.

Note: In PINE OS, this function is supported by BIOS TIMDAT.

(14) Power switch read

Function: Reads the current state of the power switch.

Sequence:



Explanation:

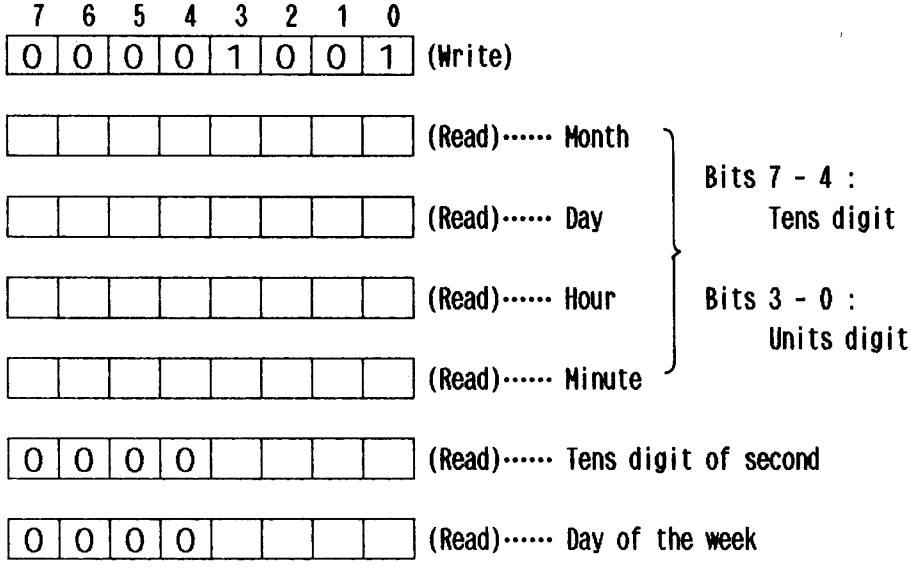
This command is used to read the ON/OFF state of the power switch on the side panel of the main unit.

Note: In PINE OS, this function is supported by BIOS READSW.

(15) Alarm read

Function: Reads the alarm time which is currently set.

Sequence:



Explanation:

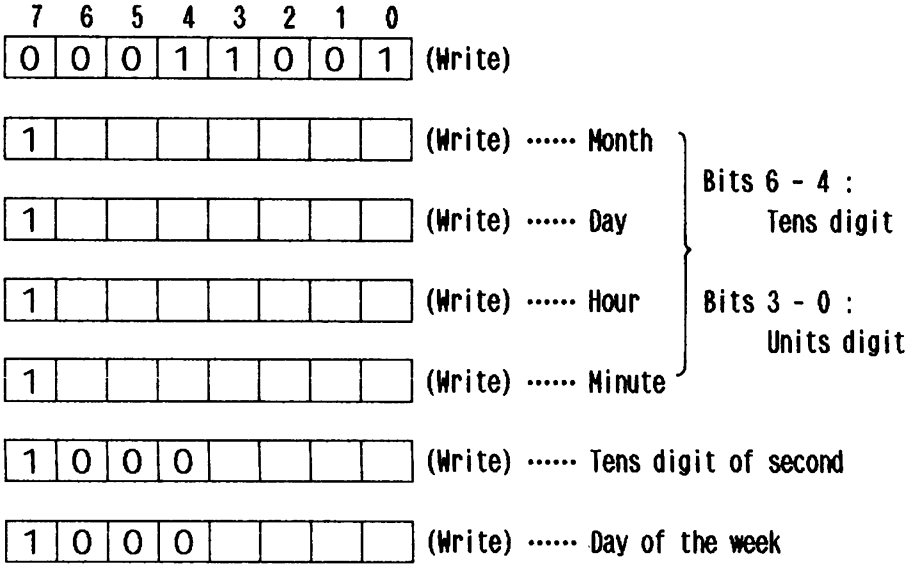
This command is used to read the month, day, hour, minute, second, and day of the week of the alarm time which is currently set. All these items are specified in BCD notation.

Note: In PINE OS, this function is supported by BIOS TIMDAT.

(16) Alarm set

Function: Sets the alarm time.

Sequence:



Explanation:

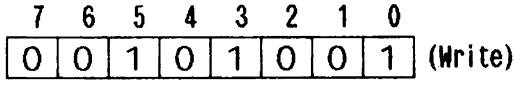
1) This command is used to specify the month, day, hour, minute, second, and day of the week for the alarm time. All these items are defined in BCD notation. The MSB of data bytes must always be set to 1.
2) It is permissible to specify an item as eight 1 bits. (For example, setting the minute field to all 1's causes alarm interrupts to be generated every minute.)
3) The year and the units digit of the second cannot be specified.
4) To enable the alarm function, command (18) must be executed after this command.

Note: In PINE OS, this function is supported by BIOS TIMDAT.

(17) Alarm off

Function: Disables alarm interrupts.

Sequence:



Explanation:

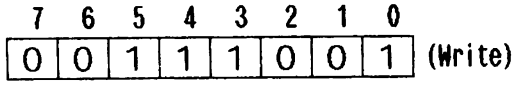
1) This command is used to disable alarm interrupts to the Z-80 CPU. Any alarm interrupts generated in alarm off state are ignored. Subsequently, these interrupts are suppressed even if the alarm state is switched to ON.
2) Alarm interrupts are disabled by default.

Note: In PINE OS, this function is supported by BIOS TIMDAT and MASKI.

(18) Alarm on

Function: Enables alarm interrupts.

Sequence:



Explanation:

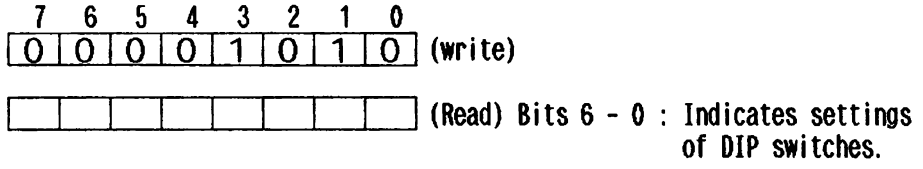
1) This command is used to enable the Z-80 CPU for alarm interrupts.
2) Alarm interrupts are generated at the alarm time specified by command (16).

Note: In PINE OS, this function is supported by BIOS TIMDAT and MASKI.

(19) DIP switch read

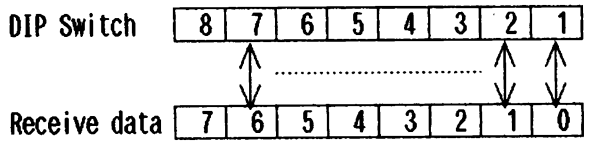
Function: Reads the settings of the DIP switches on the rear panel of the main unit.

Sequence:



Explanation:

1) The figure below shows the correspondence between the DIP switches and receive data bits.



2) In the receive data, a 1 bit indicates that the DIP switch is set to ON, and a Ø bit indicates OFF. The MSB (bit 7) indicates the keyboard type regardless of individual DIP switch settings.

MSB = 1 : Item keyboard
= Ø : Standard keyboard

Note: In PINE OS, the DIP switch bits are used to specify the following items:

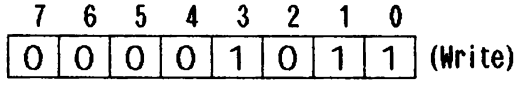
DIP switch bit 8 : Keyboard type
bits 7, 6 : LST: device
bits 4-1 : Character set setting

This function is supported by BIOS READSW.

(2Ø) STOP key interrupt disable

Function: Enables the Z-8Ø CPU for keyboard interrupts.

Sequence:



Explanation:

1) This command is used to enable the Z-8Ø CPU for keyboard interrupts.
2) This command performs the same function as command (11).

(21) STOP key interrupt enable

Function: Enables the Z-80 CPU only for STOP key interrupts and disables all other keyboard interrupts.

Sequence:

7	6	5	4	3	2	1	0	
0	0	0	1	1	0	1	1	(Write)

Explanation:

1) This command is used to enable the Z-80 CPU only for the STOP key interrupt. After this command is executed, no keyboard interrupts other than the STOP key interrupts can be generated. The key code of a pressed key is placed in the key buffer.
2) If an item keyboard is installed, sending this command leads to the same result as executing command (10). Remember that the item keyboard has a different key code system than the standard keyboard.

Note: In PINE OS, this function is used in BIOS BEEP processing and supported by BIOS MASKI.

(22) 7 chraracter buffer

Function: Sets the keyboard buffer length to 7 characters.

Sequence:

7	6	5	4	3	2	1	0	
0	0	0	0	1	1	0	0	(Write)

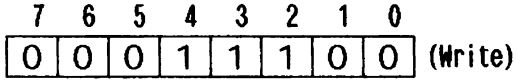
Explanation:

1) This command is used to set the 7508 keyboard buffer length to 7 characters. Unsent key data is temporarily stored in the buffer.
2) Extra key or switch codes are ignored when the buffer is full. However, the STOP key code can be added to the end of the buffer.
3) The keyboard buffer length is set to 7 characters by default.

(23) 1 chraracter buffer

Function: Sets the keyboard buffer length to 1 character.

Sequence:



Explanation:

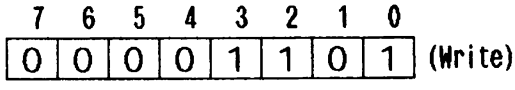
1) This command is used to set the 7508 keyboard buffer length to 1 character.
2) The 1 character buffer performs the same function as the 7 character buffer mentioned by command (22).

Note: PINE OS provides a keyboard buffer which can store up to 32 characters.

(24) 1 sec. interrupt off

Function: Disables one second interrupts.

Sequence:



Explanation:

This command is used to disable one second interrupts from the 7508. After this command is executed, the Z-80 CPU is disabled for 1-second interrupts.

Notes:

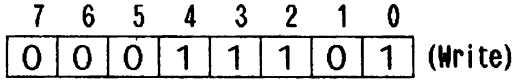
1) In PINE OS, this function is supported by BIOS MASKI.
2) In PINE OS, 1-second interrupts are used to control the clock under the following conditions:
   (1) When checking auto power-off time
   (2) When the alarm screen is displayed
   (3) When ROM cartridge power is off

   After this command is executed, the clock cannot be controlled under the conditions listed above.

(25) 1-second interrupt on

Function: Enables 1-second interrupts from the 7508.

Sequence:



Explanation:

This command is used to enable 1-second interrupts from the 7508. After this command is executed, the Z-80 CPU is enabled for 1-second interrupts.

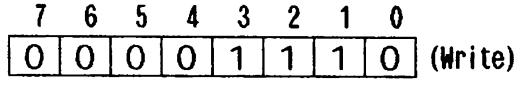
Notes:

1) In PINE OS, this function is supported by BIOS MASKI.
2) In PINE OS, this command is issued during reset processing or system initialize processing.

(26) KB clear

Function: Resets keyboard buffer data.

Sequence:



Explanation:

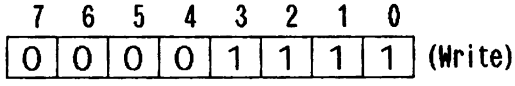
1) This command is used to clear the 7508 keyboard buffer, scan the keyboard and load information concerning the currently pressed key into the buffer.
2) This command differs from command (3). It does not initialize the keyboard status (e.g. the repeat start time).

Note: In PINE OS, this command is used to scan the key codes which were stored in the buffer before the STOP key was pressed.

(27) System reset

Function: Resets the 7508 CPU.

Sequence:



Explanation:
This command is used to reset (initialize) the 7508 CPU.

Note: This command cannot be used in application programs. The PINE starts system initialize processing when it receives a System Reset command.

CHAPTER 4 PINE INTERFACES

CHAPTER 4 PINE INTERFACES

This chapter discusses the interfaces for the following PINE facilities:

1. Cartridge
2. Serial communication facilities
3. System bus
4. Others

4.1 Cartridge Interface

4.1.1 General

The PINE is provided with a cartridge interface which interfaces to optional equipment such as the microcassette, ROM cartridge, RAM cartridge, cartridge printer, and universal cartridge. The cartridge interface operates in different modes depending on the optional unit connected. There are four cartridge interface modes: HS, IO, DB, and OT modes.

For cartridge devices, see Section 5.1, "Cartridges" in Part II "Software."

4.1.2 Cartridge Interface Modes

(1) HS mode (Hand Shake mode)
The HS mode is available for optional devices which has a processor. In this mode, data transfer is done between the input and output buffers. Handshaking is controlled by flags IBF and OBF.
(2) IO mode (Input/Output port mode)
In this mode, the cartridge interface controls transfer between a 4-bit input port and a 4-bit output port.
(3) DB mode (Data Bus mode)
This mode permits the PINE to treat the optional device as an ordinary IC device. The cartridge interface connects the main unit data bus directly to the cartridge data bus.
(4) OT mode (Output port mode)
In this mode, the cartridge interface serves as an 8-bit output port.

4.1.3 Selecting the Mode

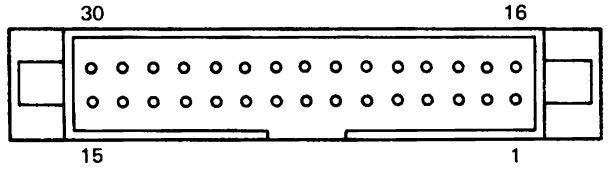
The operating mode of the cartridge interface can be selected by setting cartridge switches CSW1 and CSW0 (bits 1 and 0) of SWR (at P18H). CSW1 and CSW0 are initialized to 0 (HS mode) by an initialize routine implemented in a gate array.

CSW1	CSW0	Mode
0	0	HS mode
0	1	IO mode
1	0	DB mode
1	1	OT mode

4.1.4 Cartridge Connector Pin Assignments

The table below shows the cartridge connector pine assignments.

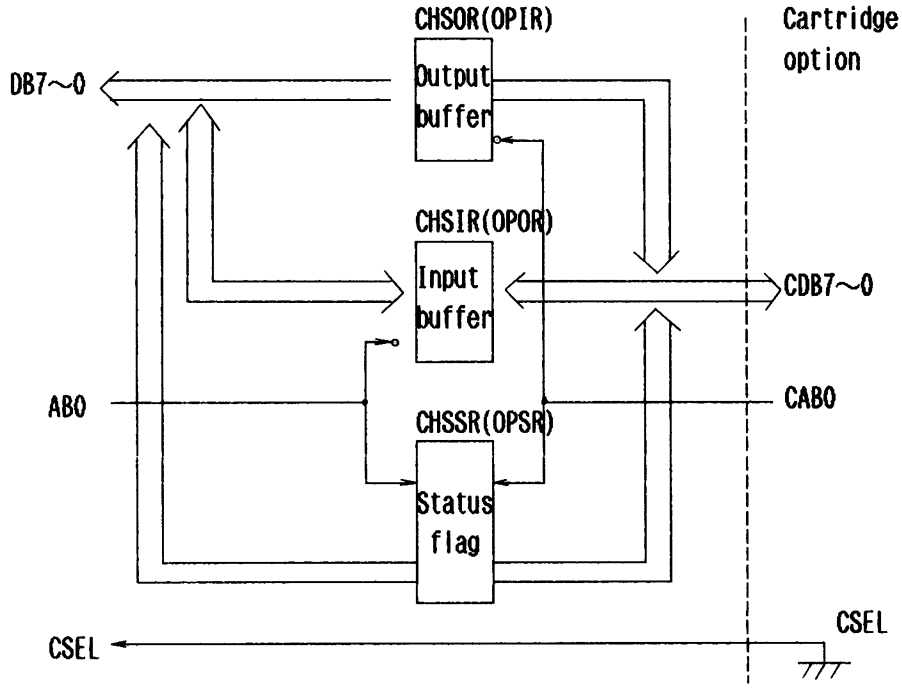
Pin No.	Name	Pin No.	Name
1	GND (ground for ±5V)	2	CAUD (audio input)
3	CDB4 (data bus)	4	$\overline{\text{CRD}}$ (read signal)
5	CDB0 (data bus)	6	$\overline{\text{CITO}}$ (interrupt)
7	$\overline{\text{CCS}}$ (chip select)	8	$\overline{\text{CRS}}$ (cartridge set)
9	CAB0 (address bus)	10	CSEL (mode select input)
11	GND (ground for VB1)	12	CDB2 (data bus)
13	VB1	14	CRXD (serial input)
15	−5V	16	+5V
17	CG (case ground)	18	CDB1 (data bus)
19	CG (case ground)	20	CAB1 (address bus)
21	FPOF	22	CDB7 (data bus)
23	CDB3 (data bus)	24	CEN
25	$\overline{\text{CWR}}$ (write signal)	26	CTXD (serial output)
27	CDB6 (data bus)	28	$\overline{\text{RS}}$ (reset)
29	CDB5 (data bus)	30	VB2



Name	H S	D B	I O	O T
CCS	(Input) Chip select input	(Output) Chip select output	Not used	Not used
CAB1	(Input) General-purpose input line	(Output) Address output	Not used	Not used
CAB0	(Input) Address input	(Output) Address output	Not used	Not used
$\overline{\text{CRD}}$ $\overline{\text{CWR}}$	(Input) Read/Write pulse	(Output) Read/Write pulse	Not used	Not used
CDB 7~0	(I/O) Data bus input/output	(I/O) Data bus input/output	(Output) Port output (CDB - 7 CDB - 4) (Input) Port input (CDB - 3 CDB - 0)	(Output) 8 - bit port output
CSEL	(Input) Selects the optional device. CSEL = 0 : HS mode cartridge = 1 : Non HS mode cartridge			
$\overline{\text{CITO}}$	(Output) Interrupt signal	Not used	Not used	Not used
CAUD	(Input) Digital audio signal to SP (loud speaker)			
CTXD	(Output) Serial transmit data line			
CRXD	(Input) Serial receive data line			
$\overline{\text{CRS}}$	(Output) Reset signal to the cartridge option, Set to 0 by an initial reset.			

(Input) = Cartridge → PINE
(Output)= PINE → Cartridge

4.1.5 HS Mode



(1) Explanation
In the HS mode, the PINE interfaces to the optional cartridge unit through an input and output buffers. When the PINE writes a byte into the output buffer, the optional unit can read it. When the optional unit writes a data byte into the input buffer, the PINE can read it. Handshaking is controlled by OBF (Output Buffer Full) and IBF (Input Buffer Full). CDB7-CDBØ, CABØ, $\overline{CRD}$, $\overline{CWR}$, and $\overline{CCS}$ are sent from the optional unit.

The cartridge interface identifies a byte sent from the PINE with ASBØ set to 1 as a command and a byte sent with ASBØ set to Ø as a data byte. The value of ABØ is latched into status flag register bit FØ. The optional unit can read this flag with a Status Read.

When a byte is written into the output buffer, whether it is a command or data byte, OBF is set to 1 and $\overline{CITØ}$ to Ø, generating an interrupt request to the optional unit. The state of OBF can be read by both the PINE and optional unit with a Status Read (the role of OBF and IBF is reversed between the PINE and optional unit; OBF viewed from the PINE is interpreted as IBF by the optional unit).

The optional unit identifies the occurrence of a data write from the PINE through an interrupt or status read and takes in the write data with the state of command/data flag FØ. OBF is reset to Ø and $\overline{CITØ}$ to 1 when the output buffer is read by the optional unit. The optional unit reads the output buffer with CABØ set to Ø and reads status with CABØ set to 1.

When the optional unit writes a byte into the input buffer (the type of data written by the optional unit is irrelevant, so the CAB0 state is a don't care. However, CAB0 is set to 0 by convention), IBF is set to 1. The PINE can tests this state with a Status Read and reads the data from the input buffer. IBF is reset to 0 by reading the input buffer. The PINE reads the input buffer with AB0 reset to 0 and reads status with AB0 set to 1.

In the HS mode, CAB1 is used as not an address line but as a general-purpose input from the optional unit. The state of CAB1 can be read by the PINE as part of status data.
When the cartridge unit is used in the HS mode, CSEL must be pulled down to the 0 level.

(2) I/O address space
The I/O address space in the HS mode is shown in the table below.

HS mode I/O address space

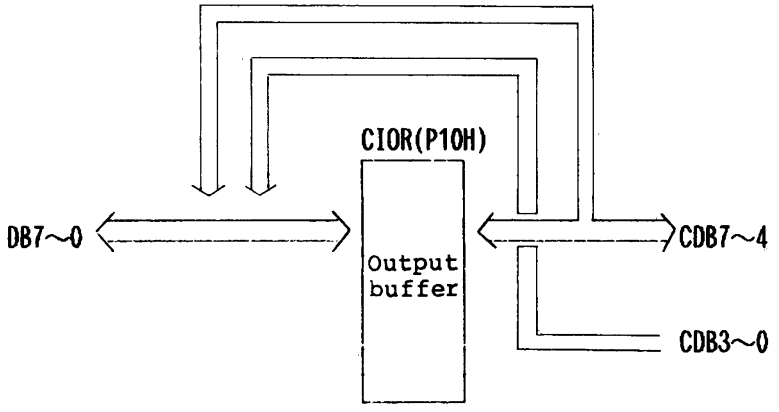
R/W	I/O address	Register Name	7 6 5 4 3 2 1 0	Flag
READ	10H	CHSIR	8 bits data	IBF reset
	11H	CHSSR	CAB1 IBF OBF	
	12H	Not used (access inhibited)		
	13H			
Write	10H	CHSOR	8 bits data	OBF set, F0=0
	11H	CHSOR	8 bits command	OBF set, F0=1
	12H	Not used (access inhibited)		
	13H			

I/O address space as viewed from the cartridge option

R/W	CAB0	Register Name	7 6 5 4 3 2 1 0	Flag
READ	0	OPIR	8 bits data	OPIBF reset
	1	OPSR	F0 OPIBF OPOBF	
WRITE	0	OPOR	8 bits data	OPOBF reset
	1		Not used (access inhibited)	

Note the following relationships:
OPIR = CHSOR OPOR = SHSIR
OPIBF = OBF OPOBF = IBF

4.1.6 IO Mode



(1) Explanation
In the IO mode, the cartridge interface consists of a 4-bit output port (CDB7-CDB4) and a 4-bit input port (CDB3-CDBØ). Output data is latched into an 8-bit latch (CIOR). Input data is read directly (without latching) into the CPU over CDB3 through CDBØ. The address of the input/output port it 1ØH.

When the PINE CPU writes output data into the port at P1ØH, the contents of the 8-bit data bus are latched into the CIOR. THe higher order 4 bits of the CIOR output are connected to CDB7 through CDB4. The lower order 4 bits of the CIOR output are not connected.

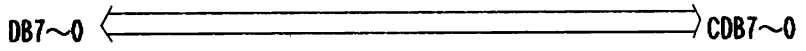
When port P1ØH is read, data from CDB3 through CDBØ are directed directly to the lower four bits of the PINE data bus. The higher order 4 bits of the data bus are loaded with the higher order 4 bits of the output buffer.

In the IO mode, CSEL must be held at the 1 level. $\overline{CCS}$, CAB1, CABØ, $\overline{CWR}$, and $\overline{CRD}$ must be held in the high impedance state, so they must be pulled up or down into the inactive state. The $\overline{CIT0}$ output is set to 1.

(2) IO address space
The IO address space in the IO mode is shown in the table below.

R/W	IO address	Register Name	7 6 5 4	3 2 1 0
READ	10H	CIOR	(Output port contents)	CDB3~0
	11H	Not used (access inhibited)		
	12H			
	13H			
WRITE	10H	CIOR	4 bits data	Don't care
	11H	Not used (access inhibited)		
	12H			
	13H			

4.1.7 DB Mode



(1) Explanation
In the DB mode, the PINE CPU handles the cartridge option as an ordinary I/O device. To the CPU, the cartridge option looks like an I/O device having four I/O addresses.

CDB7 through CDBØ are connected directly to system data bus bits DB7 through DBØ. $\overline{CCS}$, $\overline{CRD}$, $\overline{CWR}$, CAB1, and CABØ are controlled by the CPU; that is, these lines are all output lines.

$\overline{CCS}$ is set to Ø when one of I/O addresses 1ØH through 13H is selected. CAB1 and CABØ serve as the lowest 2 address bits. $\overline{CRD}$ and $\overline{CWR}$ are I/O read and write pulses generated by the CPU.

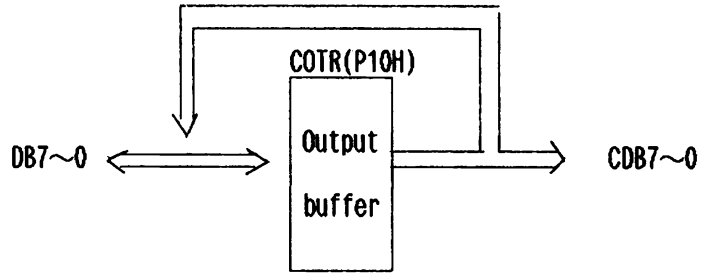
In the DB mode, CSEL must be set to 1 and the $\overline{CIT0}$ output to 1.

(2) I/O address space
The I/O address space in the DB mode is shown in the table below.

R/W	IO address	Register Name	7	6	5	4	3	2	1	0
READ	10H	Defined by the cartridge option.								
	11H									
	12H									
	13H									
WRITE	10H									
	11H									
	12H									
	13H									

Note: The higher 4 bits (bits 7-4) of P13H are used to identify the optional unit.

4.1.8 OT Mode



(1) Explanation
In the OT mode, the cartridge interface consists of an 8-bit output port (latch). The address of the output buffer (COTR) is 1ØH. When the CPU writes a data byte into port address 1ØH, the contents of the data bus (DB7-DBØ) are latched into the COTR and, simultaneously, placed on the output port pins CDB7 through CDBØ. When port 1ØH is read, the contents of the COTR are read into the CPU.

In the OT mode, CSEL must be held at the 1 level. $\overline{CCS}$, CAB1, CABØ, $\overline{CWR}$, and $\overline{CRD}$ must be held in the high impedance state, so they must be pulled up or down into the inactive state. The CITØ output is set to 1.

(2) IO address space
The IO address space in the OT mode is shown in the table below.

R/W	IO address	Register Name	7 6 5 4 3 2 1 0
READ	10H	COTR	(Output port contents)
	11H	Not used (access inhibited)	
	12H		
	13H		
WRITE	10H	COTR	8 bits data
	11H	Not used (access inhibited)	
	12H		
	13H		

Note: Physically, CHSOR, CIOR, and COTR refer to the same register.

4.1.9 Identifying the Cartridge Mode

The cartridge interface is initialized to the HS mode and CSW1 and CSWØ are set to Ø when an initial reset is performed. Simultaneously, flags (IBF and OBF) are reset to Ø. In other words, when the PINE is powered on or reset, CDB7-CDBØ, $\overline{CRD}$, $\overline{CWR}$, $\overline{CCS}$, CAB1, and CABØ are placed into the input (high impedance) state, preventing the occurrence of data conflicts even when an optional unit is connected to the cartridge interface in any mode.

The PINE OS establishes the cartridge mode, on an initial reset or when the cartridge option is replaced, all in the HS mode. To do this, the system examines CSEL. If CSEL is Ø, identifying an HS mode option, the system transfers control immediately to the corresponding option handling routine. If CSEL is 1, indicating an option other than HS mode options, the system puts the interface into the DB mode to further identify the cartridge option. In the DB mode, $\overline{CCS}$, $\overline{CRD}$, $\overline{CWR}$, CAB1, and CABØ are all designated as outputs. In the other modes, these signals are not used at all, so no output data conflict can occur. The system then reads P13H and examines the higher order 4 bits. The optional device must supply its device address on CDB7 through CDB4 so that the system can identify the type of the option.

When the system identifies a DB mode option, it transfers control immediately to the corresponding option handling routine. If the option is an IO or OT mode option, however, the system must initialize the output ports before setting up the mode. To do this, the system returns once to the HS mode, writes the initialization data into the higher order 4 bits of the CIOR or 8 bits of the COTR, then sets up the IO or OT mode.

Figure 4.1.1 shows the flowchart for setting up the cartridge mode.

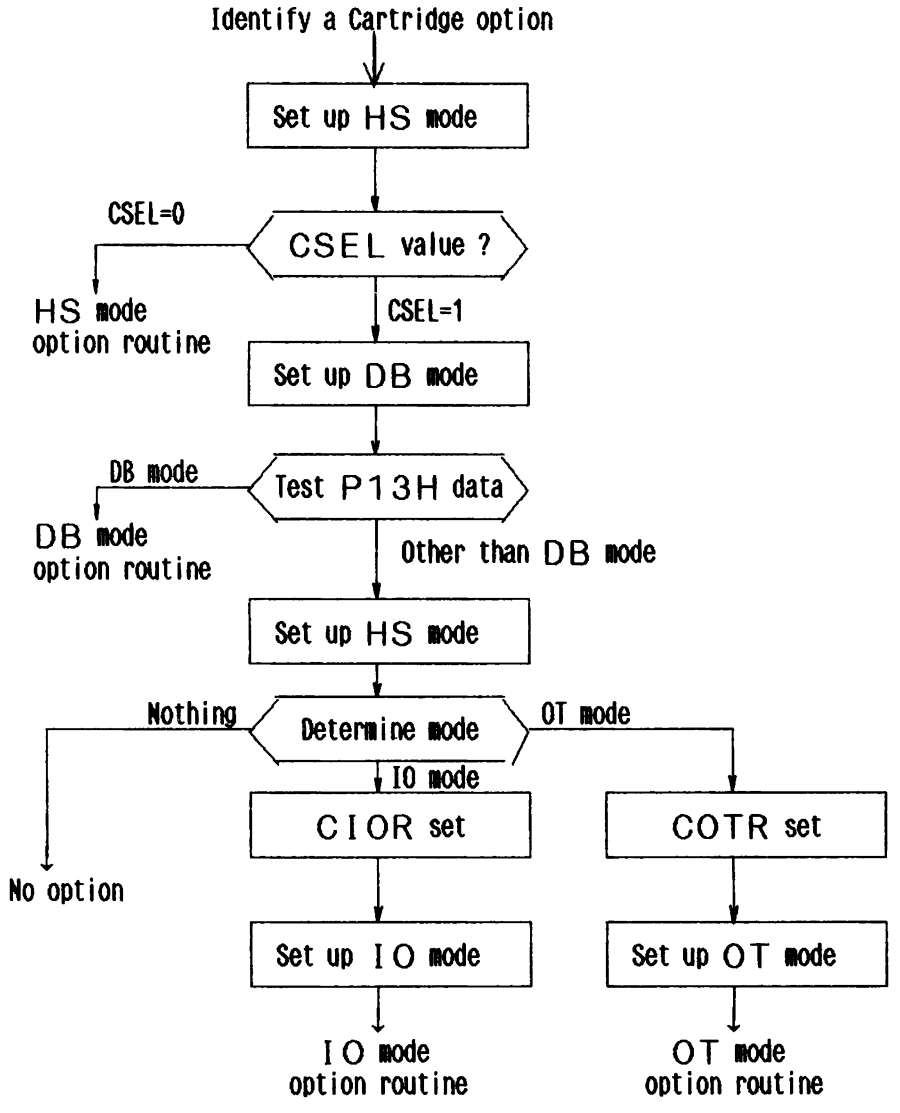


Fig. 4.1.1 Identifying a Cartridge Option

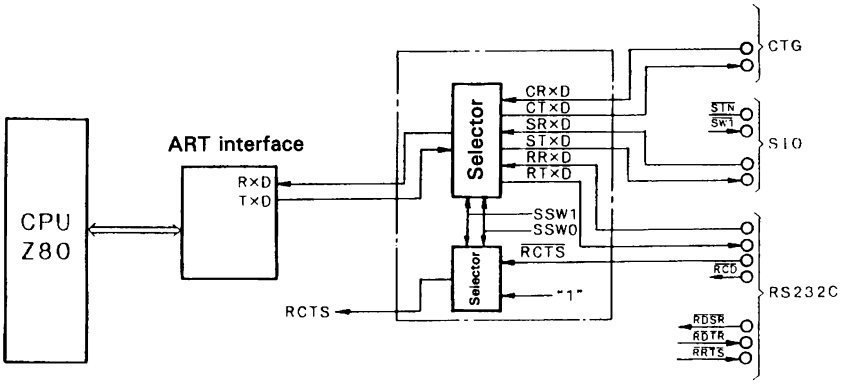
4.2 Serial Interfaces

4.2.1 General

The PINE is provided with three types of serial interfaces (RS-232C, SIO, and CTG SIO). During system operation, one of these interfaces is selected by a serial switch circuit and connected to the (8251-compatible) ART interface.

4.2.2 Serial Switch

The serial interface is selected out of the RS-232C, SIO, and cartridge SIO by select bits SSW1 and SSWØ of SWR (bits 3 and 2). The serial interface block diagram is shown below, followed by a table showing the relationship between the serial interfaces and the values of SSW1 and SSWØ.



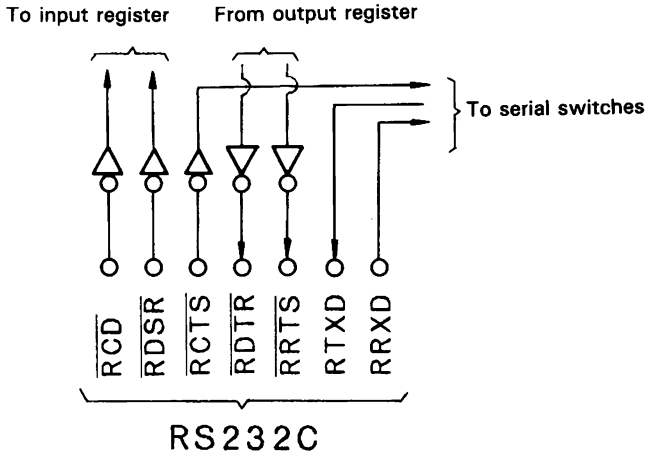
Serial mode	SSW1	SSW0	RXD	TXD	RCTS
0	0	0	(CTG) CRXD	(CTG) CTXD	1
1	0	1	(SIO) SRXD	(SIO) STXD	1
2	1	0	(RS-232C)RTXD	(RS-232C)RTXD	Inverted signal of $\overline{\text{RCTS}}$
3	1	1	(RS-232C)RRXD	(SIO) STXD	Inverted signal of $\overline{\text{RCTS}}$

Serial mode 3 is a special mode in which data is received from the RS-232C interface and sent to the SIO interface. CTXD, STXD, and RTXD are held high (mark level) when not selected.

4.2.3 RS-232C Interface

The RS-232C interface has two data lines (RRXD and RTXD) and three control inputs ($\overline{RCD}$, $\overline{RCTS}$, and $\overline{RDSR}$) and two control output ($\overline{RRTS}$ and $\overline{RDTR}$). RRXD and RTXD are connected to the ART through serial switches. The state of $\overline{RCD}$, $\overline{RCTS}$, and $\overline{RDSR}$ can be read by reading IOSTR bits 4, 5, and ARTSR bit 7, respectively. These signals use negative logic and their state is inverted before being input to the main CPU which uses positive logic. This means that when the signal at a RS-232C terminal is Ø, the corresponding register bit is set to 1.

$\overline{RCTS}$ behaves in different ways depending on the value of serial switches SSW1 and SSWØ. $\overline{RDTR}$ and $\overline{RCTS}$ are the inverted outputs of ARTCR bits 1 and 5. When these bits are set to 1, the corresponding bits at the RS-232C interface are set to Ø.



The RS-232C signals as read by the main CPU from the registers, those at the GAPNIO gate array pins, and those at the RS-232C connector differ in polarity. The polarity of these signals is summarized in the table below.

Signal name	Register	GAPNIO	Connector	Initial value (register bit, GAPNIO pin)
RRXD Receive Data	Note 1	RRXD +	$\overline{\text{RRXD}}$ −	
RTXD Transmit Data		RTXD +	$\overline{\text{RTXD}}$ −	
RRTS Request To Second	ARTCR 5 +	$\overline{\text{RRTS}}$ −	RRTS +	0. 1
RDTR Data Terminal Ready	ARTCR 1 +	$\overline{\text{RDTR}}$ −	RDTR +	0. 1
RCTS Clear To Send	IOSTR 5 +	$\overline{\text{RCTS}}$ −	RCTS +	
RDSR Data Set Ready	ARTSR 7 +	$\overline{\text{RDSR}}$ −	RDSR +	
RCD Carrier Detect	IOSTR 4 +	$\overline{\text{RCD}}$ −	RCD +	

\+ : positive
− : negative

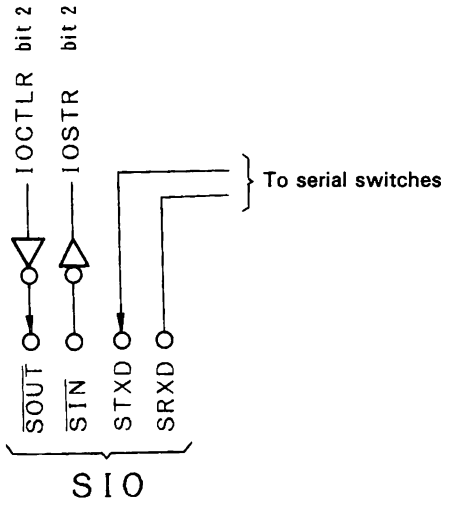
Note 1: The state of RRXD can be obtained by reading IOSTR bit 3 when SSW1 is set to 1.

4.2.4 SIO Interface

The SIO interface is a simplified version of the RS-232C interface. It has two data lines (SRXD and STXD) and two control lines ($\overline{SIN}$ and $\overline{SOUT}$).

SRXD and STXD are connected to the ART through serial switches. $\overline{SIN}$ is an inverted signal of IOSTR bit 2. For example, IOSTR bit 2 is 1 when $\overline{SIN}$ pin is set to Ø. $\overline{SOUT}$ corresponds to IOCTLR bit 2. It is set to Ø when IOCTLR bit 2 is set to 1.

The state of SRXD can be obtained by reading IOSTR bit 3 in serial mode 1.



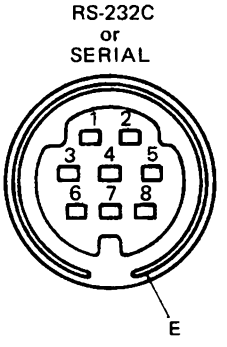
4.2.5 Connectors

(1) RS-232C

Pin No.	Description
1	GND (Ground)
2	$\overline{RTX}$ (Transmit Data)
3	$\overline{RRX}$ (Receive Data)
4	RTS (Request to Send)
5	CTS (Clear to Send)
6	DSR (Data Set Ready)
7	DTR (Data Terminal Ready)
8	CD (Carrier Detect)
E	CG (Frame Ground)

(2) SIO

Pin No.	Description
1	GND (Ground)
2	$\overline{STX}$ (Transmit Data)
3	$\overline{SRX}$ (Receive Data)
4	
5	
6	SIN (Status Input)
7	SOUT (Control Output)
8	
E	CG (Frame Ground)



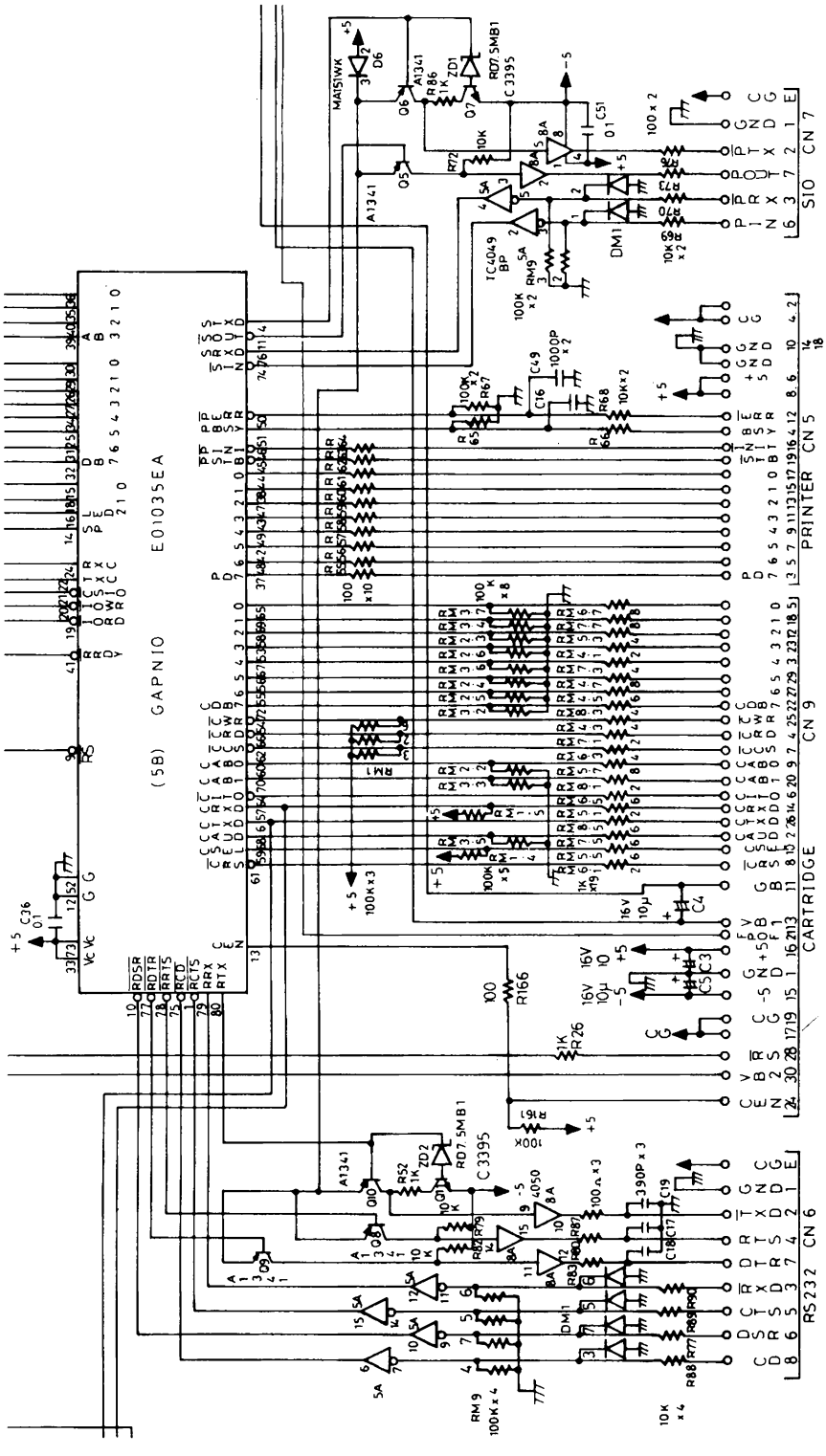


Fig. 4.2.1 Cartridge Interface Circuit Diagram

4.3 System Bus

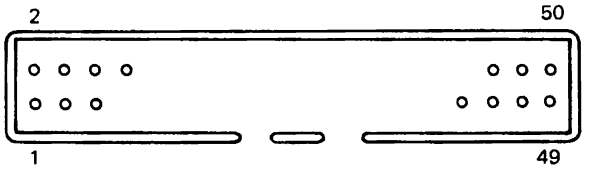
4.3.1 General

The PINE system bus connects to the external RAM disk option. The PINE OS uses I/O port 94H to identify the presence of the external RAM disk unit. This port address must not be used by the user when an external unit other than RAM disk units is connected.

4.3.2 Connector Pin Assignments

Pin	Description	Pin	Description
1	VCH (charge power, 7.8~ 8.8V)	2	VB1 (4.8~ 6.5V, 300mA)
3	VB2 (PW.ON : 5V, 15mA) (PW.OFF: 4.8-6.5V, 0.5mA)	4	VBK (internal battery, 4.8V)
5	GND (VL)	6	VL (5V, 70mA)
7	DB7 (Data bus)	8	DB6 (Data bus)
9	DB5 (Data bus)	10	DB4 (Data bus)
11	DB3 (Data bus)	12	DB2 (Data bus)
13	DB1 (Data bus)	14	DB0 (Data bus)
15	$\overline{MEN}$ (External memory select)	16	$\overline{INTE}$ (Interrupt input)
17	$\overline{WAIT}$ (Wait)	18	$\overline{PON}$ (Power On signal)
19	$\overline{CLK}$ (System clock)	20	CTXD/BUSAK
21	$\overline{RD}$ (Read)	22	$\overline{IORQ}$ (I/O request)
23	$\overline{WR}$ (Write)	24	$\overline{MRQ}$ (Memory Request)
25	$\overline{HLTA}$ (Halt acknowledge)	26	CRXD/BUSRQ
27	CG (Frame ground)	28	CG (Frame ground)
29	$\overline{RS}$ (Reset)	30	$\overline{M1}$ (Machine cycle 1)
31	AB0 (Address bus)	32	AB1 (Address bus)
33	AB2 (Address bus)	34	AB3 (Address bus)
35	AB4 (Address bus)	36	AB5 (Address bus)
37	AB6 (Address bus)	38	AB7 (Address bus)
39	AB8 (Address bus)	40	AB9 (Address bus)

41	AB10 (Address bus)	42	AB11 (Address bus)
43	AB12 (Address bus)	44	AB13 (Address bus)
45	AB14 (Address bus)	46	AB15 (Address bus)
47	OFF (Off signal)	48	DW (Refresh control)
49	DCAS (Refresh control)	50	$\overline{\text{RSI}}$ (Reset input)



PON: Generated by the slave CPU to activate the DC-to-DC converter. This line is battery backed up.
OFF: Held at the high level when power is off and used to switch the PINE from the memory backup state to the power-on state. This line is controlled by the slave CPU and battery backed up.
$\overline{\text{CLK}}$: Is the 3.6864 MHz system clock.
$\overline{\text{RS}}$: System reset signal. This line is battery backed up.
$\overline{\text{RSI}}$: Setting this line low generates a reset signal to the PINE CPU.
DCAS: Used by the system bus side to set the PINE into the self-refresh mode. This line is battery backed up.
DW: Same as above.
$\overline{\text{MEN}}$: When this line is held low, the main CPU can access the ROM or RAM in the main unit. When this line is set high by the system side, the main CPU can access the ROM or RAM on the system bus side. In this case, the RAM in the main unit is undergo memory refreshing and the main CPU can access the I/O registers with no problem.
$\overline{\text{WAIT}}$: WAIT input from the system bus.
$\overline{\text{INTE}}$: Interrupt enable signal from the system bus.

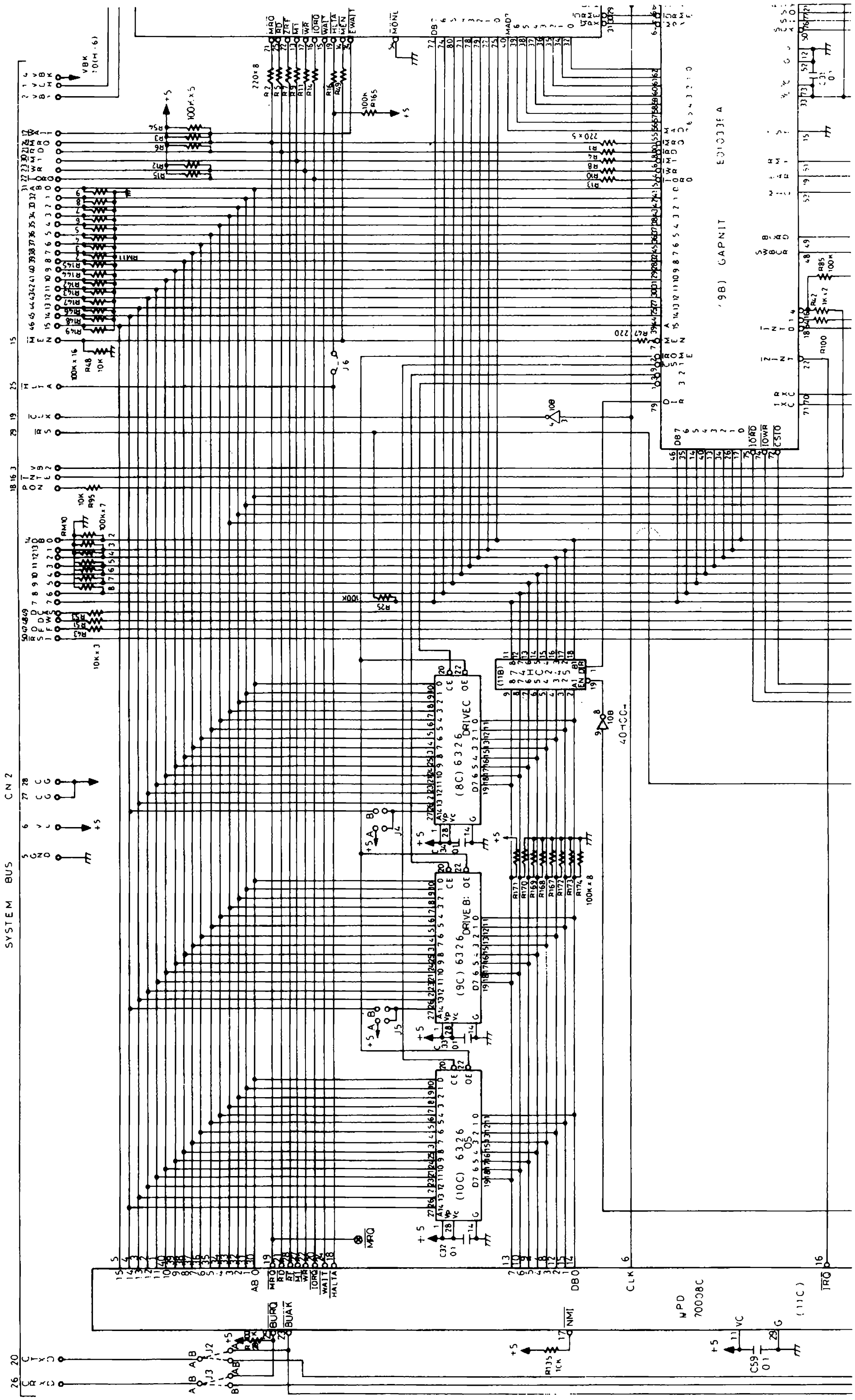


Fig. 4.3.1 System Bus Circuit Diagram

4.4 Other Interfaces

4.4.1 General

This section describes the Printer, loudspeaker, external cassette, and barcode interfaces.

4.4.2 Printer Interface

The Centronics interface is an 8-bit parallel interface which interfaces the PINE to one of the EPSON standard printers. It uses $\overline{\text{PSTB}}$ strobe output and PBSY busy input for handshaking. It has also $\overline{\text{PERR}}$ which indicates printer error status and $\overline{\text{PINI}}$ which initializes the printer. Including data lines, the Centronics interface has a total of 12 signal lines.

(1) Block diagram
Figure 4.4.1 shows the Centronics interface block diagram.

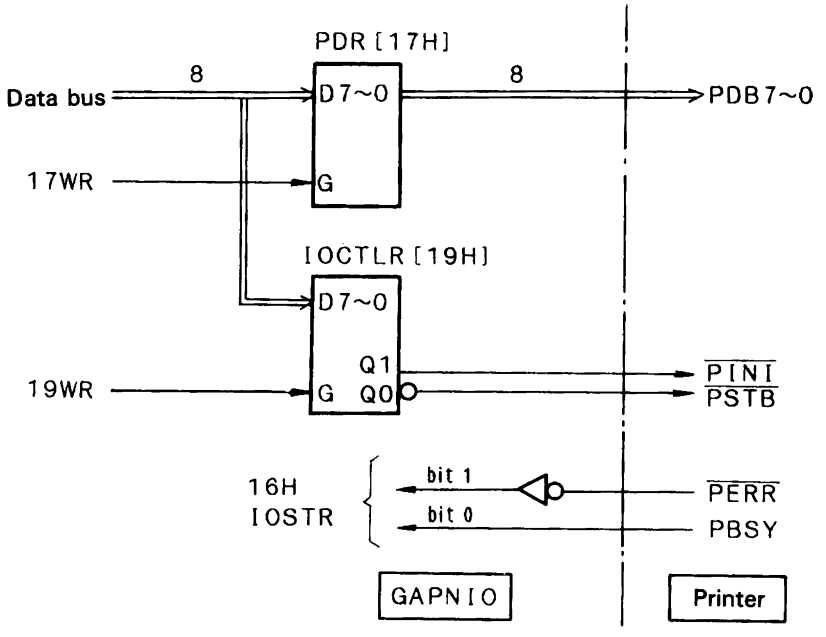
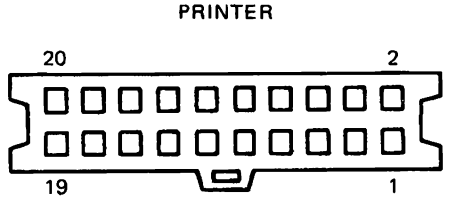


Fig. 4.4.1 Printer Interface Block Diagram

(2) Connector

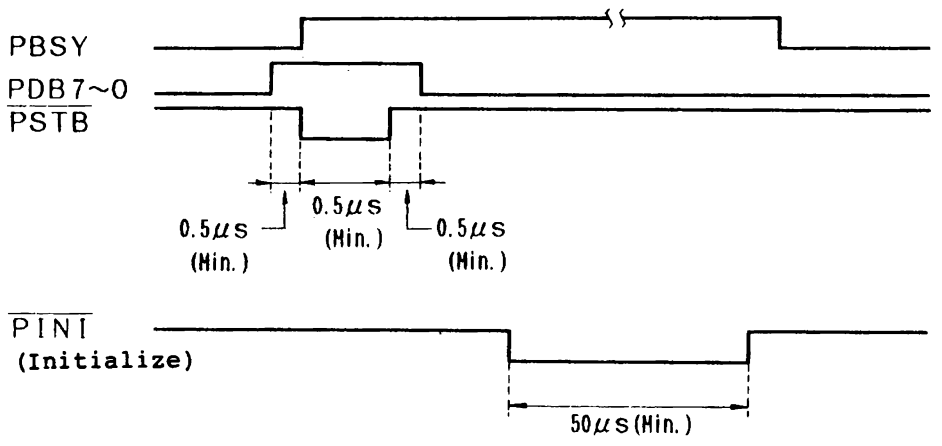
Pin	Description	Pin	Description
1	CG (Frame ground)	2	CG (Frame ground)
3	PDB7 (Print data)	4	PBSY (Busy signal)
5	PDB6 (Print data)	6	+5V
7	PDB5 (Print data)	8	+5V
9	PDB4 (Print data)	10	GND (Ground)
11	PDB3 (Print data)	12	$\overline{\text{PERR}}$ (Error signal)
13	PDB2 (Print data)	14	GND (Ground)
15	PDB1 (Print data)	16	$\overline{\text{PINIT}}$ (Reset signal)
17	PDB0 (Print data)	18	GND (Ground)
19	$\overline{\text{PSTB}}$ (Strobe signal)	20	NC



(3) Relationship between register bits and interface pins

pin name	Main unit to printer	Logic	Description	Register bit	Explanation
PDB7~0	→	Positive	8-bit parallel data	[17H] PDR	Writing is into register bits sets the corresponding. PDB pins to 1. PDR can not be initialized.
$\overline{\text{PSTB}}$	→	Negative	Data strove signal with a pulse width of 0.5us minimum. This signal is low active and normally held high.	[19H] IOCTLR bit0 • PSTB	Writing a 1 into IOCTLR bit 0 (PSTB) sets the PSTB pin to 0. Initially, the PSTB bit is reset and the $\overline{\text{PSTB}}$ pin is set to 1.
$\overline{\text{PINI}}$	→	Negative	Initializes the printer controller. This signal has minimum pulse width of 50us. It is active low and normally held high.	[19H] IOCTLR bit1 • $\overline{\text{PINI}}$	Writing a 1 into IOCTLR bit 1 (PINI) sets the $\overline{\text{PINI}}$ pin to 0. The PINI pinis set to 0 by an initial reset.
PBSY	←	Positive	A high in this bit indicates that the printer is busy and cannot receive print data.	[16H] IOSTR bit0 • PBSY	The PBSY register bit is set to 1 when the PSSY pin is set to 1.
$\overline{\text{PERR}}$	←	Negative	A low in this bit indicates that the printer is in an error state.	[16H] IOSTR bit1 • PERR	The $\overline{\text{PERR}}$ register bit is set to 1 when the PSSY pin is set to 0.

(4) Timing chart



4.4.3 Loudspeaker Interface

The loudspeaker interface controls the output signal to the loudspeaker. It inputs the audio signal (CAUD) from the cartridge interface and the SP signal (IOCTLR bit 7) that is set by the CPU and outputs the loudspeaker output.

A switch named AUSW (SWR bit 4) is provided which turns on and off the CAUD signal to the loudspeaker. When this switch is 1, the CAUD signal is passed to the loudspeaker.

(1) Block diagram
Figure 4.4.2 shows the loudspeaker block diagram.

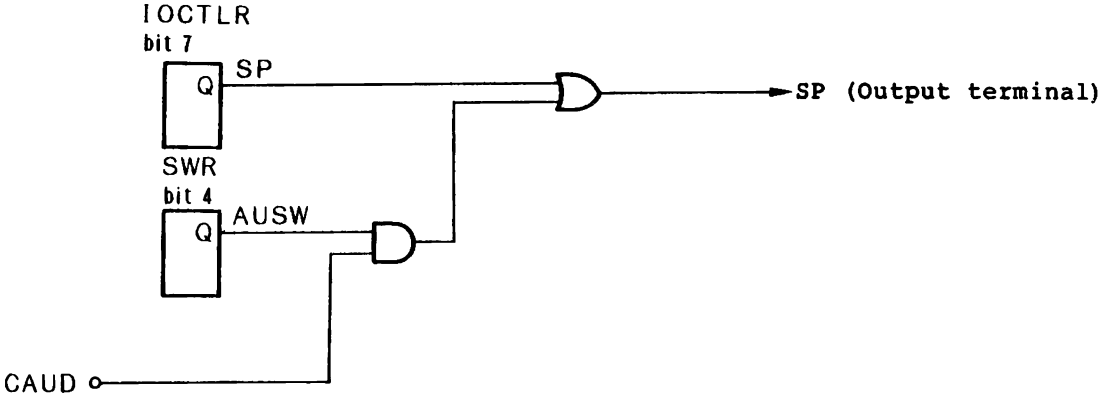


Fig. 4.4.2 Loudspeaker Block Diagram

(2) Loudspeaker signal states
The table below shows the relationship between the SP, AUSW, and CAUD signals.

SP (IOCTLR bit 7)	AUSW (SWR bit 4)	CAUD	Speaker output terminal
0	1	(CAUD)	CAUD
(SP)	0	*	SP
0	0	*	0
(SP)	1	(CAUD)	CAUD+SP

The following four types of signals can be output to the loudspeaker:

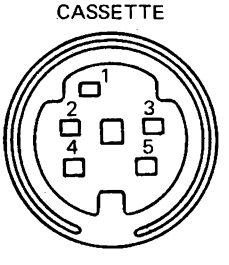
1. CAUD
2. SP
3. Ø
4. Superimposition of CAUD and SP

PINE OS generates beep sounds by turning on and off SP; it does not control the AUSW bit.

4.4.4 Miscellaneous Interface Signals

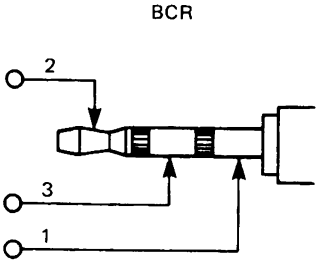
(1) External cassette

Pin No.	Name	
1	GND	(Ground)
2	RMT	(Remote output)
3	RMT	(Remote output)
4	MIC	(Microphone output)
5	EAR	(Earphone input)
E		



(2) Barcode reader

Pin No.	Name	
1	GND	(Ground)
2	BRD	(Barcode data)
3	+5V	(Power source)



(3) External buzzer

Pin No.	Name
1	GND (Ground)
2 , 3	EX
10	SP