Part III INTERFACE

Contents

Chapter 1 Outline

Chapter 1 Outline

1.1 Outline of PINE Hardware

The PINE uses CMOS-ICs. The main CPU is a CMOS type Z-8Ø operating with a clock frequency of 3.6864 MHz. Electrical characteristics of this CPU are the same as those of a NMOS type Z-8Ø CPU.
Three custom LSIs are used in the main interface circuits and the registers in these LSIs are controlled by using I/O instructions. The user can access these registers by using the BASIC OUT and INP statements.
The cartridge interface is controlled by LSI called GAPNIO. This LSI operates in one of the four interface modes which is selected according to the operation required. The I/O addresses 1ØH to 13H are assigned to GAPNIO and the addresses used for I/O operation differ according to the interface mode.
The PINE operating system checks the device address to know the device connected to the cartridge interface. This port is always accessed when the main CPU reset status is released.
When the user sets the device address, data bus lines CDB4 to CDB7 must be pulled up via resistance. The PINE OS does not recognize any addresses other than those for its cartridges.
The contents of registers are lost when the power is turned off.
To use the system bus to connect a user's interface circuit, I/O addresses 2ØH to FFH can be used. The PINE OS read address 94H to check the existence of the external RAM disk. Therefore, do not use this address for the user's interface.
There are other interfaces which can be used by the user. Using the bar code reader interface makes it mpossible to measure the pulse width and frequency of the input signal. Therefore, connecting a sensor to this interface makes it possible to perform automatic measurement.
The system bus and cartridge interface can be used for serial communication as well as the RS-232C and serial interfaces. Using these interfaces enables to make a new type of communication system.
Since the printer interface consists of I/O registers only, the user can use it if the printer is not used. In this case, set the DIP switches to other than the printer position.
The external cassette tape recorder remote output terminals are internally connected to the relay contacts so that these output terminals can be used to control external electronic devices. These relay contact can be controlled by using the BASIC MOTOR statement or by accessing resister RMT (Ø2W).
Although the maximum current of these relay contacts is 3 A, use it at 24 V, Ø.5 A or so. The relay used is OMRON G2P-114P 3A (resistor loaded).
The PINE can be operated on the uninterruptible power supply basis by using both batteries and optional AC adapter.
The PINE can operate continuously for more than one year when optional NiCd batteries are used on the floating charge basis. Use the NiCd batteries when using an option device, such as the cartridge printer or microcassette drive, which consumes a large current. Use the NiCd batteries when using the external RAM disk.
Power can be supplied to interfaces from the main unit, however care shoukld be paid to the capacity of the power supply.
Some signal lines of interfaces are connected to the backup power supply. Therefore, interfaces must be designed so that unnecessary current should not flow when the power is off. This also applies to user designed circuits which are to be backed up.
Use flat cable connectors for connecting cables to the system bus and printer interface. The connector type used by EPSON is:

HU-500S2D-L13T manufactured by Daiichi Denshi Kogyo
The maximum length of the cable connected to the system bus is 15 cm.
The connector type connected to the cartridge interface is:
PICL-30S-LT manufactured by Nihon Koukuu Denshi Kogyo
An optional universal cartridge is available.
The connector type used for the serial and RS-232C interfaces is:
TCP8000 series manufactured by Hoshi Denki Seizo
External devices other than the standard ones should meet the standard relating to radio interference of the country where the system is used.

1.2 I/O Addresses

I/O Address	R (bits) 7	6	5	4	3	2	1	0	W (bits) 7	6	5	4	3	2	1	0	Device
00	ICRL-C Input Capture Register Low Command Trigger (8)								CTLR1 Control Register 1 (3)								GAPNIT
	8 bits data								BRG3	BRG2	BRG1	BRG0	SWBCR	BCR1	BCR0	SLBCR	
01	ICRH-C Input Capture Register High Command Trigger (8)								CMDR Command Register (3)								
	8 bits data													reset OVF	reset RDYSIO	set RDYSIO	
02	ICRL-B Input Capture Register Low Bar Code Trigger (8)								CTLR2 Control Register 2 (2)								
	8 bits data														RMT	MIC	
03	ICRH-B Input Capture Register High Bar Code Trigger (8)																
	8 bits data																
04	ISR Interrupt Status Register (5)								IER Interrupt Enable Register (5)								
				EXT	OVF	ICF	RxRDY	7508				EXT	OVF	ICF	RxRDY	7508	
05	STR Status Register (8)								BANKR Bank Register (6)								
	BANK3	BANK2	BANK1	BANK0	RDYSIO	RDY	BCRD	EAR	BANK3	BANK2	BANK1	BANK0	EDU	ECA	CKSW1	CKSW0	
06	SIOR Serial I/O Register (8)								SIOR Serial I/O Register (8)								
	8 bits data								8 bits data								
07																	
08									VADR VRAM Start Address Register (5)								GAPNDL
									A15	A14	A13	A12	A11				
09									YOFF Y Offset Register (7)								
									DSP		Y5	Y4	Y3	Y2	Y1	Y0	
0A									FR Frame Register (4)								
													F3	F2	F1	F0	
0B									SPUR Speed Up Register (6)								
										PRE2	PRE1	PRE0		POST2	POST1	POST0	
0C 0F																	
10	CTG IF (Cartridge Interface) Address Area								CTG IF (Cartridge Interface) Address Area								GAPNIO
11																	
12																	

I/O Address	R 7	6	5	4	3	2	1	0 (bits)	W 7	6	5	4	3	2	1	0 (bits)	Device
13	CTG IF (Cartridge Interface) Address Area								CTG IF (Cartridge Interface) Address Area								GAPNIO
14	ARTDIR ART Section: Data Input Register							(8)	ARTDOR ART Section: Data Output Register							(8)	
	7/8 bits data								7/8 bits data								
15	ARTSR ART Section: Status Register							(7)	ARTMR ART Section: Mode Register							(4)	
	RDSR		FE	OE	PE	TX empty	RX RDY	TX RDY	STOP		EVEN	PEN		DATE			
16	IOSTR I/O Status Register							(8)	ARTCR ART Section: Command Register							(6)	
	CAUD	CSEL	RCTS	RCD	RXD	SIN	PERR	PBSY			RRTS	ER	SBRK	RXE	RDTR	TXE	
17									PDR Print Data Register							(8)	
									8 bits data								
18									SWR Switch Register							(5)	
												AUSW	SSW1	SSW0	CSW1	CSW0	
19									IOCTLR I/O Control Register							(8)	
									SP	LED2	LED1	LED0	$\overline{CRS}$	SOUT	$\overline{PIN1}$	PSTB	
1A 1F																	
20 FF	Available																

The status of write registers can be known by reading the following addresses.

CTRL1	F001H
IER	F53EH
BANKR	F53DH
VADR	F295H
YOFF	F2A0H
DSP	EFB6H
ARTMR	F003H
ARTCR	F004H
SWR	F005H
IOCTLR	F006H

1.3 I/O registers

1.3.1 Registers in GAPNIT

Adress	Name	Contents
ØØR	ICRL.C	The lower 8 bits of the 16-bit free running counter can be read via this register.
Ø1R	ICRH.C	The higher 8 bits of the 16-bit free running counter can be read via this register.
Ø2R	ICRL.B	The lower 8 bits of the 16-bit free running counter at the time when the status of the bar code data or external cassette data changes can be read via this register.
Ø3R	ICRH.B	The higher 8 bits of the 16-bit free running counter at the time when the status of the bar code data or external cassette data changes can be read via this register.
Ø4R	ISR	Interrupt request status bit 4 EXT External interrupt bit 3 OVF Timer overflow flag bit 2 ICF Input capture flag bit 1 RXRDY Receive data ready interrupt from GAPNIO bit Ø 75Ø8 Interrupt from 75Ø8
Ø5R	STR	Status register bits 7-4 BANK 3-Ø Bank switch status bit 3 RDYSIO FF Status of RSYSIO in 75Ø8 interface bit 2 RDY RDY input from 75Ø8 bit 1 BCRD bar code reader data input bit Ø External cassette EAR input
Ø6R	SIOR	75Ø8 interface SIO register
ØØW	CTLR1	Control register bits 7-4 BRG 3-Ø Specifies baud rate of baud rate generator bit 3 SWBCR Bar code reader power switch bits 2,1 BCR1,Ø Specifies the trigger polarity of bar code reader data or external cassette tape data. bit Ø SLBCR Selects bar code reader data or external cassette tape data.
Ø1W	CMDR	Command register bit 2 reset OVF Resets overflow flag. bit 1 reset RDYSIO Resets RDYSIO FF. bit Ø set RDYSIO Sets RDYSIO FF.
Ø2W	CTLR2	Control regsiter bit 1 RMT Switches external cassette motor ON and OFF. bit Ø MIC Write data to the external cassette tape

Ø4W	IER	Interrupt enable See ISR.
Ø5W	BANKR	Bank switch and timer base clock switch bits 7-4 BANK3-Ø Bank switch bit 3 EDU Developing board switch bit 2 EXA Developing board switch bit 1,Ø CKSW1,Ø Clock switch Sets these switches according to the clock frequency (2.45 MHz, 3.Ø7 MHz or 3.68 MHz).
Ø6W	SIOR	7508 interface SIO register

1.3.2 Registers in GAPNDL

Address	Name	Description
Ø8W	VADR	Specifies the location of VRAM in DRAM.
Ø9W	YOFF	Y offset register bit 7 DSP Display ON/OFF bits 5-Ø Y5-Ø Specifies scroll condition.
ØAW	FR	Determines LCD frame frequency.
ØBW	SPUR	Controls LCD power supply impedance.

1.3.3 registers in GAPNIO

Address	Name	Description
1Ø - 13R	CTGIF	Input to cartridge interface
14R	ARTDIR	Compatible to 8251 recive buffer
15R	ARTSR	Compatible to 8251 status register (subset)
16R	IOSTR	Status input bit 7 CAUD Audio input from cartridge connector bit 6 CSEL Option ID input from cartridge connector bit 5 RCTS CTS input bit 4 RCD CD input bit 3 RXD Serial data input bit 2 SIN Control input from serial interface bit 1 PERR Error status from printer interface bit Ø PBSY Busy status from printer interface
1Ø - 13W	CTGIF	Output to cartridge interface
14W	ARTDOR	Compatible to 8251 transmit buffer

15W	ARTMR	Compatible to 8251 mode register (subset)		
16W	ARTCR	Compatible to 8251 command register (subset)		
17W	PDR	Data output to printer interface		
18W	SWR	Mode switch		
		bit 4	AUSW	Masks CAUD input from cartridge interface
		bits 3,2	SSW1,Ø	Switches serial modes.
		bits 1,Ø	CSW1,Ø	Switches cartridge modes.
19W	IOCTLR	Control and port output		
		bit 7	SP	Speaker output
		bits 6-4	LED2-Ø	LED outputs
		bit 2	SOUT	Control output to serial interface
		bit 1	$\overline{\text{PINI}}$	Initial output to printer interface
		bit Ø	PSTB	Strobe output to printer interface
		bit 3	$\overline{\text{CRS}}$	Reset signal to cartridge interface

Chapter 2 Interfaces

Chapter 2 Interfaces

2.1 Cartridge Interface

The PINE cartridge interfce connector can be connected to an optional microcassette tape drive, ROM cartridge, RAM cartridge, cartridge printer, or unversal cartridge.

2.1.1 Modes

Since each optional device uses a different type of interface circuit, the cartridge interface has various operating modes and one of the modes is selected according to the type of interface circuit connected. The modes in which the cartridge interface operates are as follows:
(1) HS mode (Handshake mode)
This is the mode selected when a device connected has its own CPU (e.g. microcassette tape drive). This mode is similar to the 8255 handshake mode in which data is transferred via the input and output buffers and data transfer is controlled by flags.
(2) IO mode (input/output mode)
The upper 4 bits of the data bus are used for the output port and the lower 4 bits for the input port.
(3) DB mode (data bus mode)
In this mode, the optional device connected is handled as a standard I/O device. The data bus of the main unit is directly connected to the data bus of the cartridge connected. In the DB mode, 4 addresses (10H to 13H) are used. This mode is used for the ROM and RAM cartridges.
(4) OT mode (output port mode)
All 8 bits of the data bus are used for the output port.

2.1.2 Mode setting

The cartridge interface opeating mode is determined by cartridge switches CSW1 and CSW0 (bits 1 and 0) of the switch register (SWR, address 18H).
These switches are initially set by the PINE OS as CSW1=1 and CSW0=0 (DB mode).

CSW1	CSW0	Mode
0	0	HS mode
0	1	IO mode
1	0	DB mode
1	1	OT mode

* When setting a mode, first set the HS mode, then set the desired mode.

2.1.3 I/O addresses

I/O addresses for IO mode

R/W	I/O address	Register	D7 6 5 4 3 2 1 0
R E A D	10	CIOR	Contents of_output_port | CDB3-0
	11		
	12	Not used (access inhibited)	
	13		
W R I T E	10	CIOR	4-bit data |
	11		
	12	Not used (access inhibited)	
	13		

I/O addresses for DB mode

R/W	I/O address	Register	D7 6 5 4 3 2 1 0
R E A D	10	Defined according to the optional device connected	
	11		
	12	Device address	
	13		
W R I T E	10		
	11		
	12		
	13		

I/O addresses for OT mode

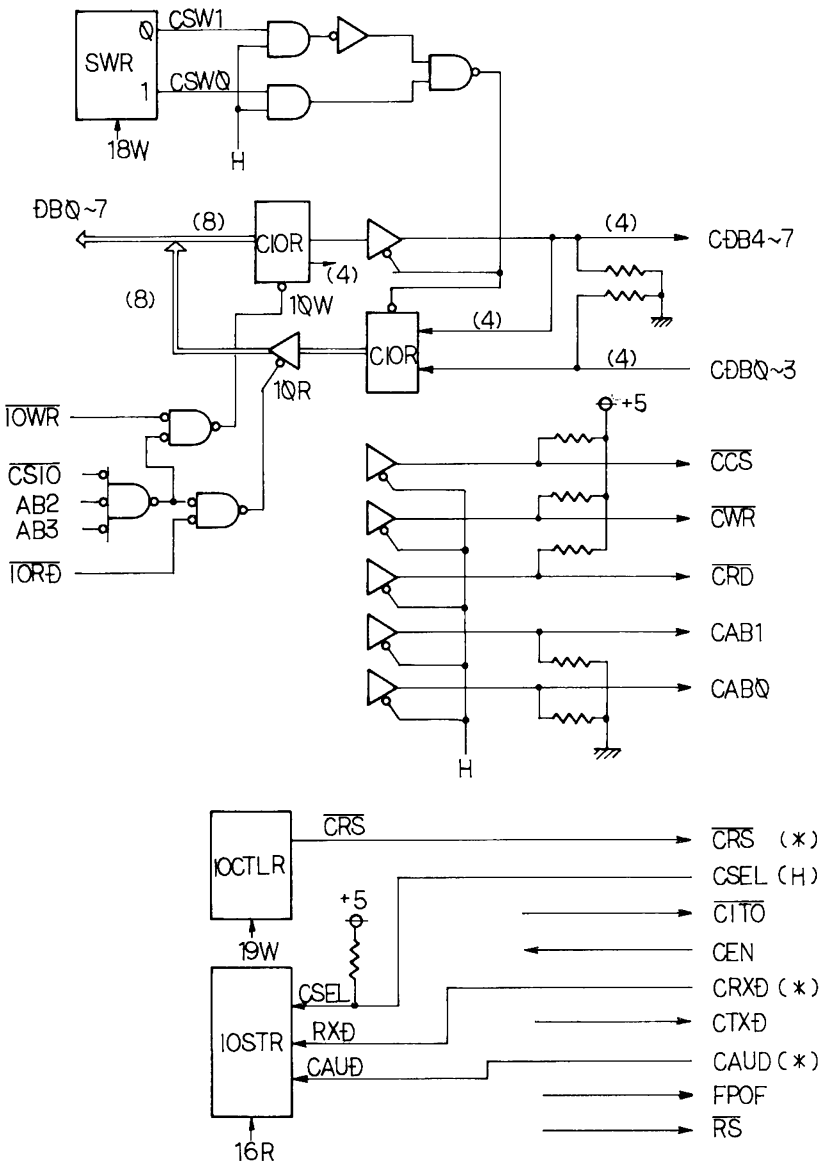
R/W	I/O address	Register	D7 6 5 4 3 2 1 0
R E A D	10	COTR	Contents of output port
	11		
	12	Not used (access inhibited)	
	13		
W R I T E	10	COTR	8-bit data
	11		
	12	Not used (access inhibited)	
	13		

Device address

CSEL	13H read 7 6 5 4	Mode Option
0		HS Microcsst
1	0 0 0 1	DB ROM crtg
1	0 0 1 0	DB RAM crtg
1	0 1 0 0	None
1	1 0 0 0	DB PROM wrtr
1	1 1 1 1	None
1	0 0 0 0	

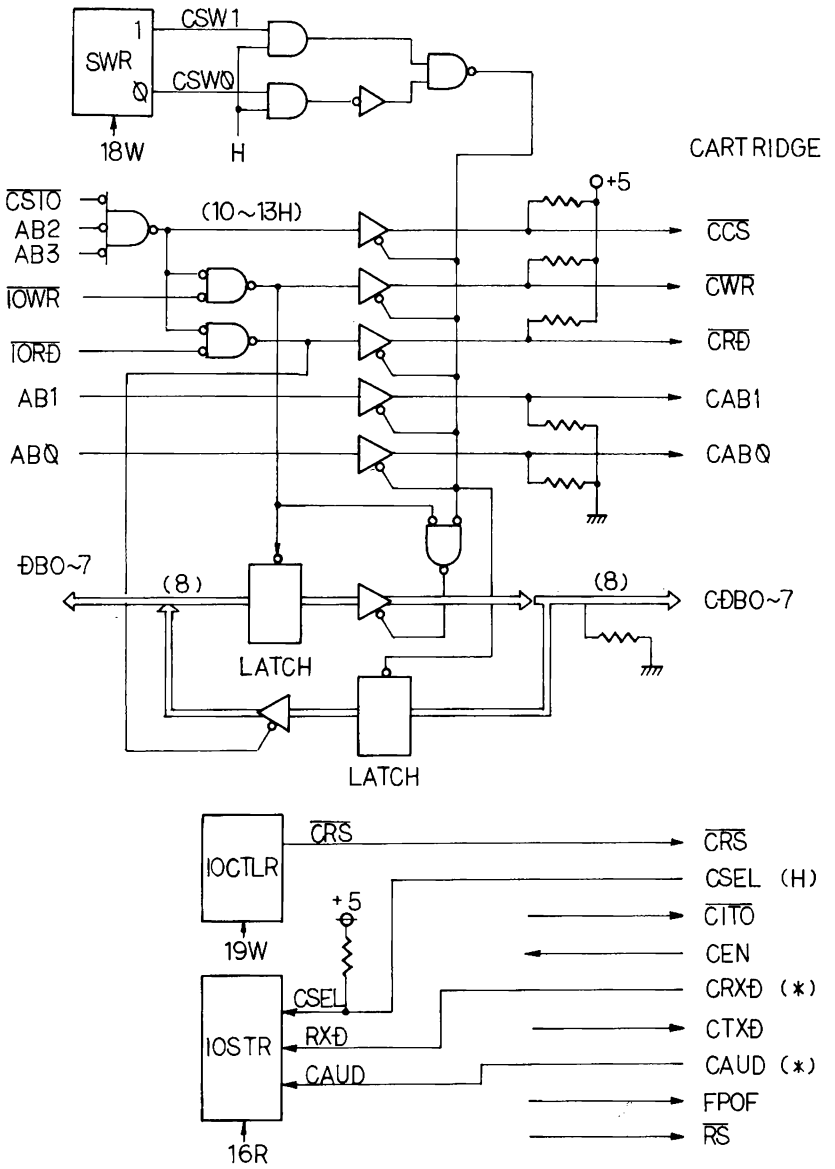
2.1.4 IO mode interface

(*) --- General purpose input/output



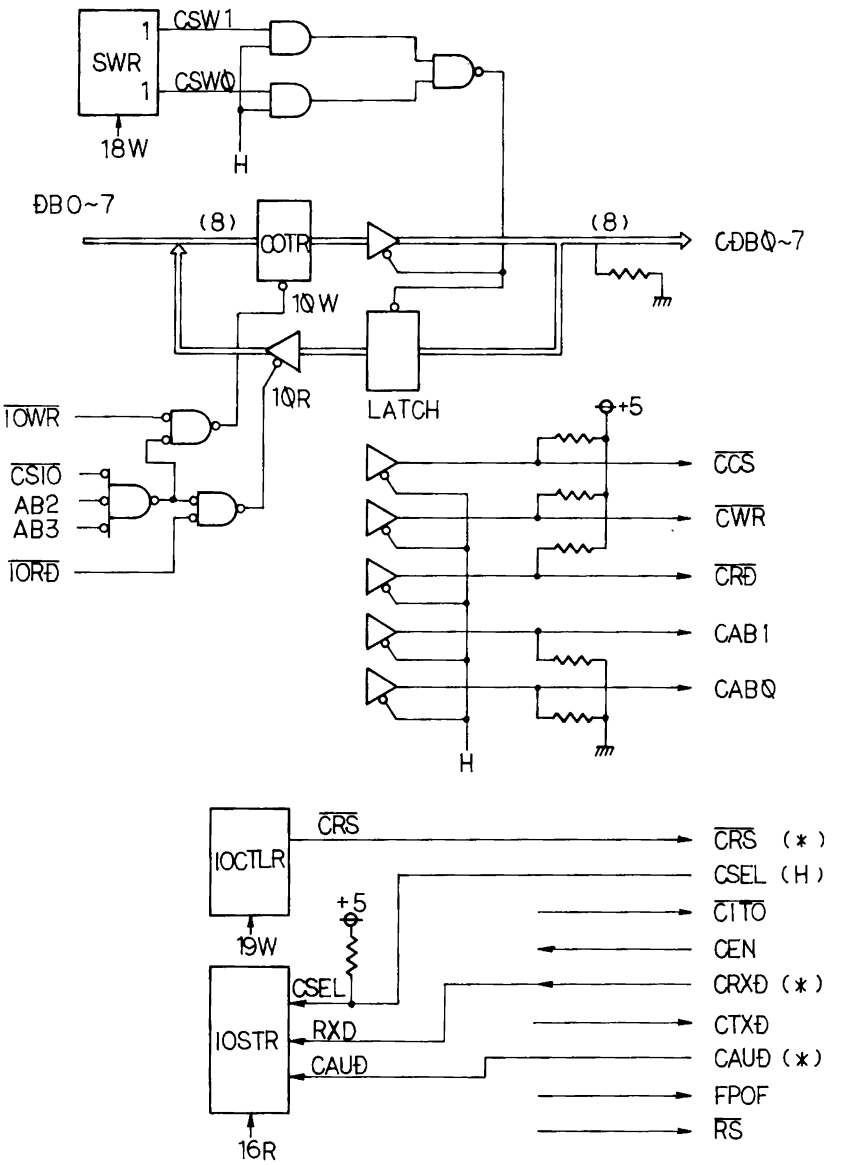
2.1.5 DB mode interface

(*) --- General purpose input/output



2.1.6 OT mode interface

(*) --- General purpose input/output



2.1.7 Sample programs

BASIC test programs for the interfaces shown in the previous pages are listed below.

IO mode interface test program
This program firat set data in register CIOR, then reads the status of the register. As a result, pulse signals are output to CDB4 to CDB7.

```
10  OUT &H18, &H01
20  OUT &H10, &HF0
30  PRINT INP(&H10)
40  OUT &H10, &H00
50  PRINT INP(&H13)
60  GOTO 20
```

0 and 240 are displayed when this program is run.

OT mode interface test program
This program outputs pulse signals to CDB0 to CDB7.

```
10  OUT &H18, &H03
20  OUT &H10, &HFF
30  PRINT INP(&H10)
40  OUT &H10, &H00
50  PRINT INP(&H10)
60  GOTO 20
```

0 and 255 are displayed when this program is run.

DB mode interface test program
This program outputs data to CDB0 to CDB7, then reads the device address and displays it.

```
10  OUT &H18, &H02
20  OUT &H13, &HFF
30  PRINT HEX$(INP (&H13))
40  GOTO 20
```

0 is displayed when this program is run.
Note: These program can be executed when no external circuit is connected to the cartridge interface. When an external circuit is connected, set the HS mode before setting the interface mode at line 10.

The status of write register cannot be read into the main CPU. Therefore, the operating system stores the data written to the register in main memory.
When setting the interface mode, the status of the switch register can be known by reading memory address F005H.

The following program shows an example which sets the mode during execution of an application program. As shownbelow, the HS mode must be set before setting the IO mode.

```
10  SWR=PEEK(&HF005)
20  CSW=SWR AND &H1C
30  POKE &HF005, CSW
40  OUT &H18, CSW
50  CSW=CSW OR &H01
60  POKE &HF005, CSW
70  OUT &H18, CSW
80  END
```

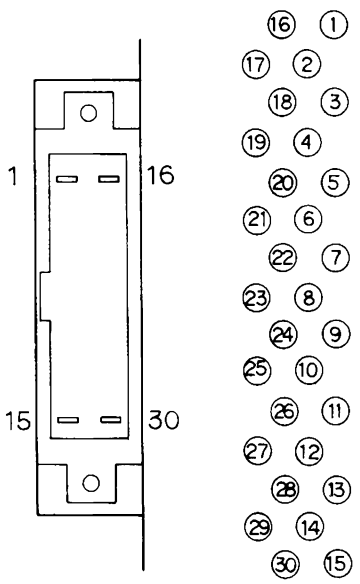
2.1.8 Cartridge connector pin functions

Signal	Explanation
$\overline{CCS}$	Chip select input from the cartridge option (HS mode). Chip select output to the cartridge option (DB mode). Not used (OT and IO modes)
CAB1	General purpose input from the cartridge option (HS mode). Address output (DB mode). Not used (OT and IO modes).
CAB0	Address input from the cartridge option (HS mode). Address output to the cartridge option (DB mode). Not used (OT and IO modes)
$\overline{CRD}$ $\overline{CWR}$	Read/write pulse input from the cartridge option (HS mode) read/write pulse output to the cartridge option (DB mode)
CDB7-0	Data bus (input/output) (HS and DB modes). 8-bit output port (OT mode). CDB7-4 for output port and CDB3-0 for input port (IO mode).
CSEL	Input from cartridge (all modes). This signal is used to identify the type of cartridge option. CSEL=0: HS mode option CSEL=1: Other mode option The status of this signal can be read as bit 6 of IOSTR.
$\overline{CITO}$	Interrupt signal used in the HS mode only. When the main unit places data or command in the output buffer, OBF becomes 1 and CITO becomes 0 so that an interrupt request is issued to the cartridge option. This request status is reset when the cartridge option reads the output buffer contents.
CAUD	Digital audio signal input connected to the speaker (all modes). Since the status of this signal can be read as bit 7 of IOSTR, this input can be used for any other purpose.
CTXD CRXD	(All modes) Data transmit and receive lines. These lines are connected to ART through the serial switch. Since the status of CRXD can be read as bit 3 of IOSTR, it can be used for any other purpose. (In this case, set as SSW1=0 and SSW0=0.)
CRS	(All modes) Reset signal to the cartridge option. This signal is set to 0 (or 1) by writing 0(or 1) to bit 3 of IOCTLR. CRS is initially set to 0. This line can be used for any other purpose if the cartridge option does not require any reset signal in the OT or IO mode.
CEN	Terminal E of 6301 is connected to this line when the cartridge uses a CPU6301. In other cases, hold this line to H.

VB1	Power supply to the cartridge printer or microcassette tape drive.
FPOF	This signal becomes H when VB1 drops and the sub-batteries are connected to the main batteries. This signal is output in the case of the worst power failure condition, so the system stops operation when this signal is detected.
RS	System reset signal This signal resets the main CPU. This signal is battery backed up and kept low even if power is turned off.
VB2	Memory backup power supply
CG	Connected to the shielding sheet under the printed circuit board. This line is connected to GND in the power supply circuit.

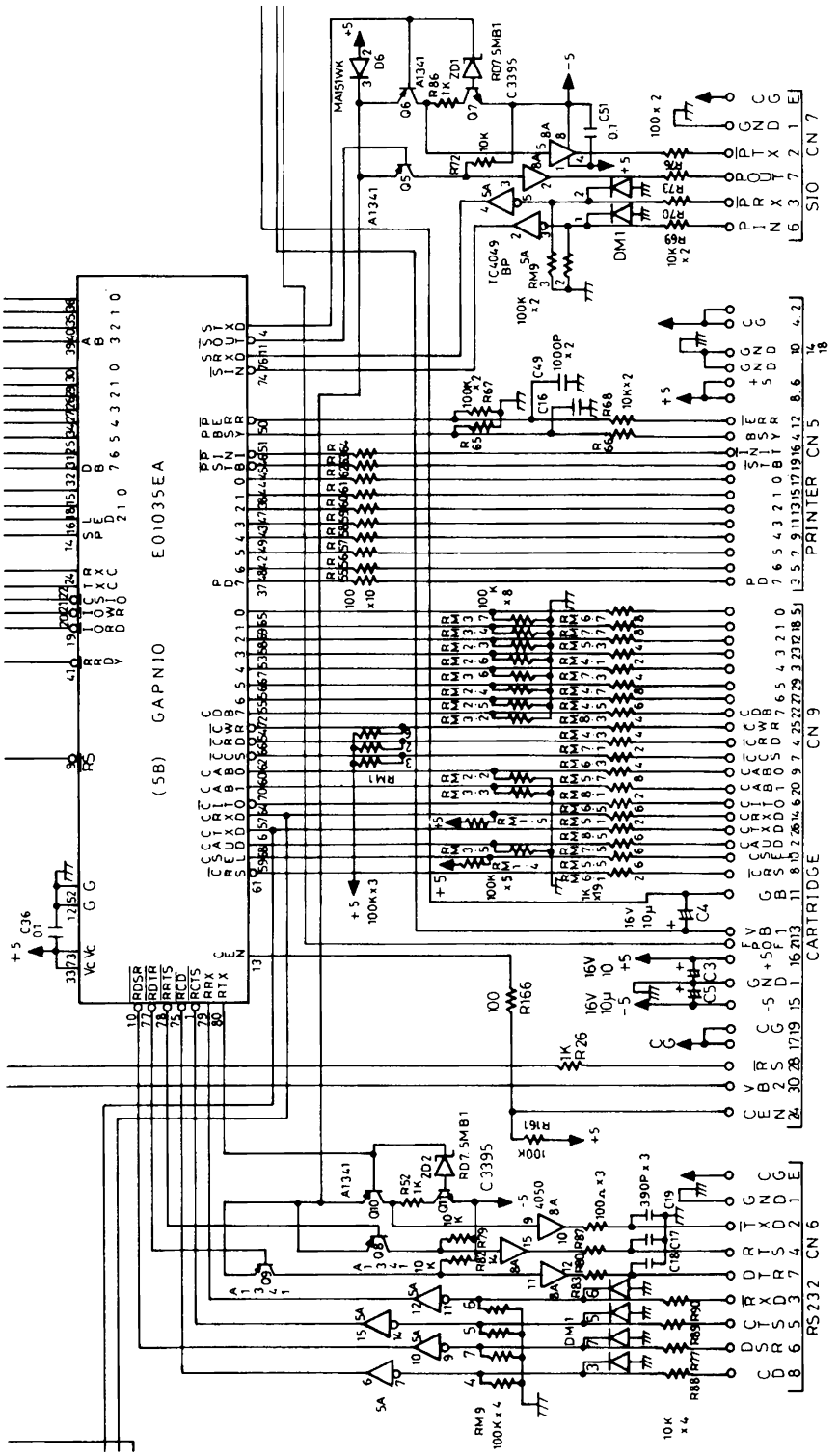
* Pins used for general purpose
  general output: $\overline{CRS}$
  general input: CAB1, CAUD, CRXD
Note the conditions under which the pin can be used for general purpose.

Connector PICL-30S-LT



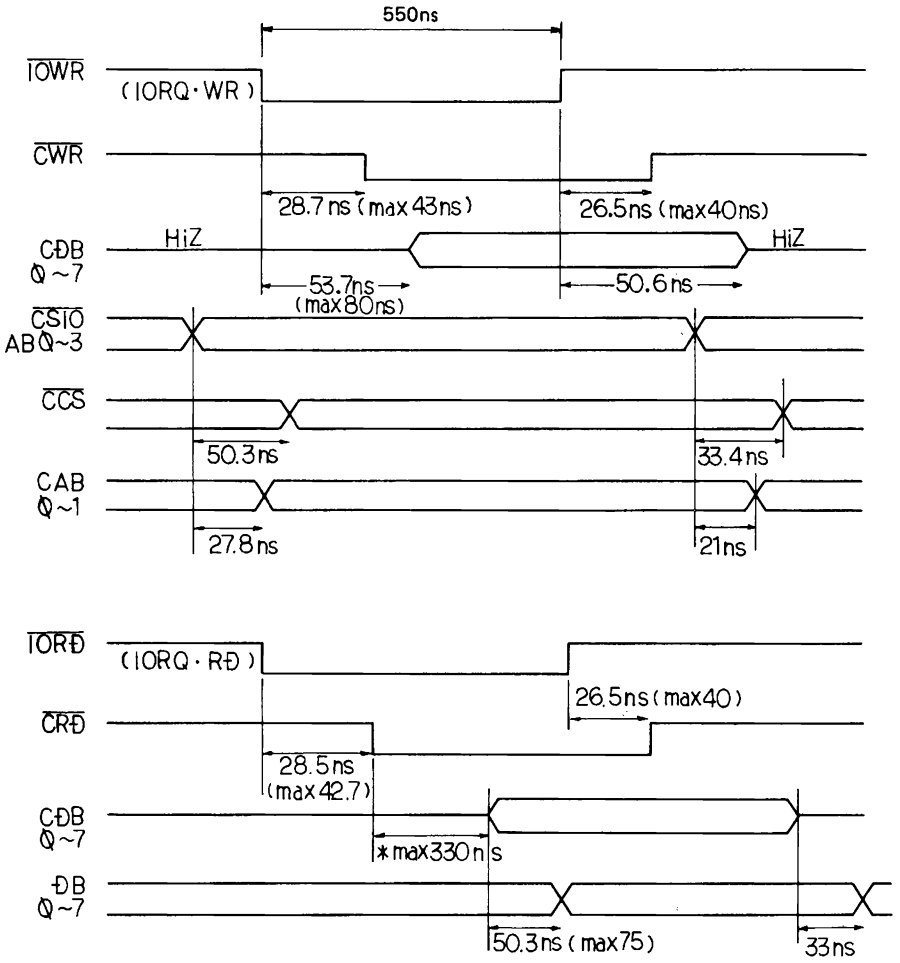
GND	1	16	+5V
CAUD	2	17	CG
CDB4	3	18	CDB1
$\overline{CRD}$	4	19	CG
CDB0	5	20	CAB1
$\overline{CITO}$	6	21	FPOF
$\overline{CCS}$	7	22	CDB7
$\overline{CRS}$	8	23	CDB3
CAB0	9	24	CEN
CSEL	10	25	$\overline{CWR}$
GB	11	26	CTXD
CDB2	12	27	CDB6
VB1	13	28	$\overline{RS}$
CRXD	14	29	CDB5
-5V	15	30	VB2

2.1.9 cartridge interface circuit

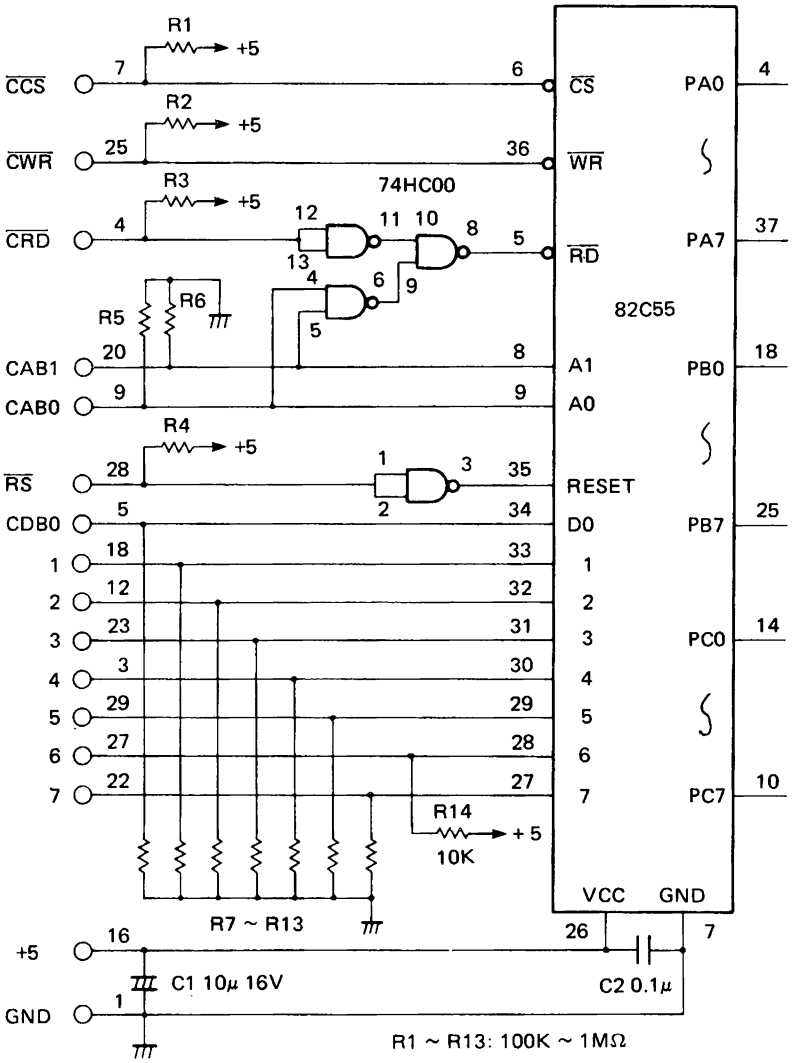


2.1.10 I/O signal characteristics (DB mode)

* The value is determined by the device connected.



2.1.11 Application circuit example

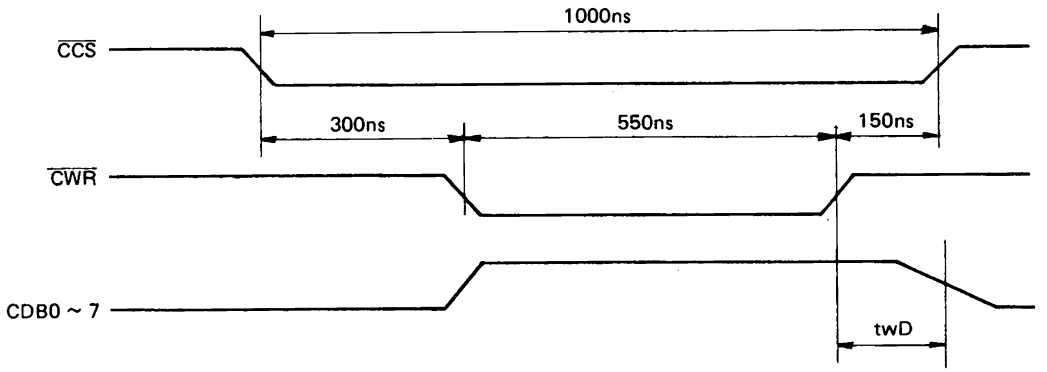


This example connects a 82C55 to the interface operating in the DB mode. If you make this circuit, be sure to check operation before use.
The PINE OS reads I/O address 13H to check the device address. Since 82C55 should not be accessed when the device address is read, the $\overline{CRD}$ signal is connected to RD of 82C55 via a gate which is closed when address 13H is accessed. This prevents 82C55 from accidentally accessed when address 13H is specified.
The device address is set by pulling up appropriate pins among CDB4 through CDB7 to +5 V with resistors (10-20 kohm).
This example set the device address to 40H.
The $\overline{CCS}$, $\overline{CWR}$ and $\overline{CRD}$ signals are output to this circuit when any of I/O addresses 10H to 13H is specified.
In the DB mode, data on lines CDB0 to CDB7 are valid only while $\overline{CWR}$ is output. This means that data hold time is too short when $\overline{CWR}$ rises from L to H. However, data is hold for an enough time because of high impedance of data lines. The timing chart shows this.
The maximum allowable delay of data output to the falling edge of $\overline{CRD}$ is 330 ns.
If the PINE OS turns power off in the continue mode, a reset signal is output to 82C55, so that application programs cannot be restarted in the continue mode. The method to restart application programs in the continue mode is explained in Chapter 3.

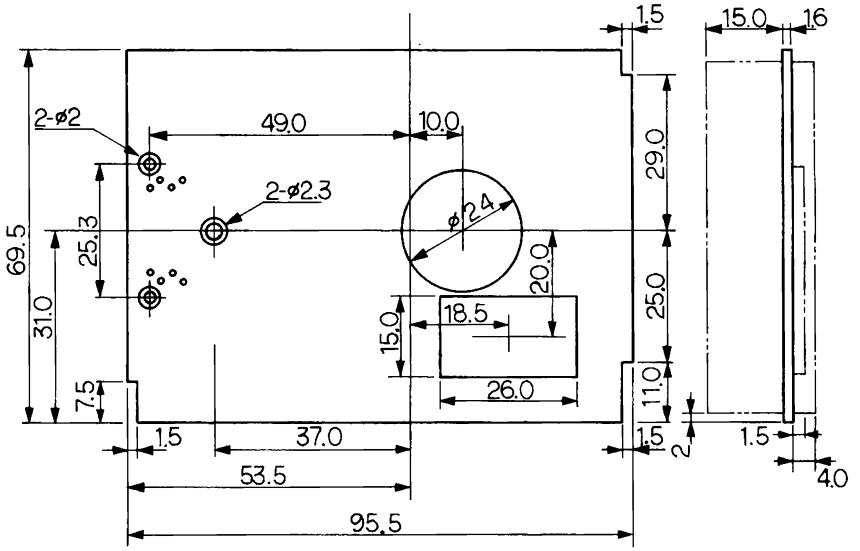
Test program

```
10 PRINT HEX$(INP(&H13))
20 OUT &H13,&H80
30 OUT &H10,&HFF
40 OUT &H10,&H00
50 GOTO 30
60 END
```

Basic output signal timing chart



2.1.12 Dimensions of unversal cartridge board
Unit: mm



2.2 System Bus

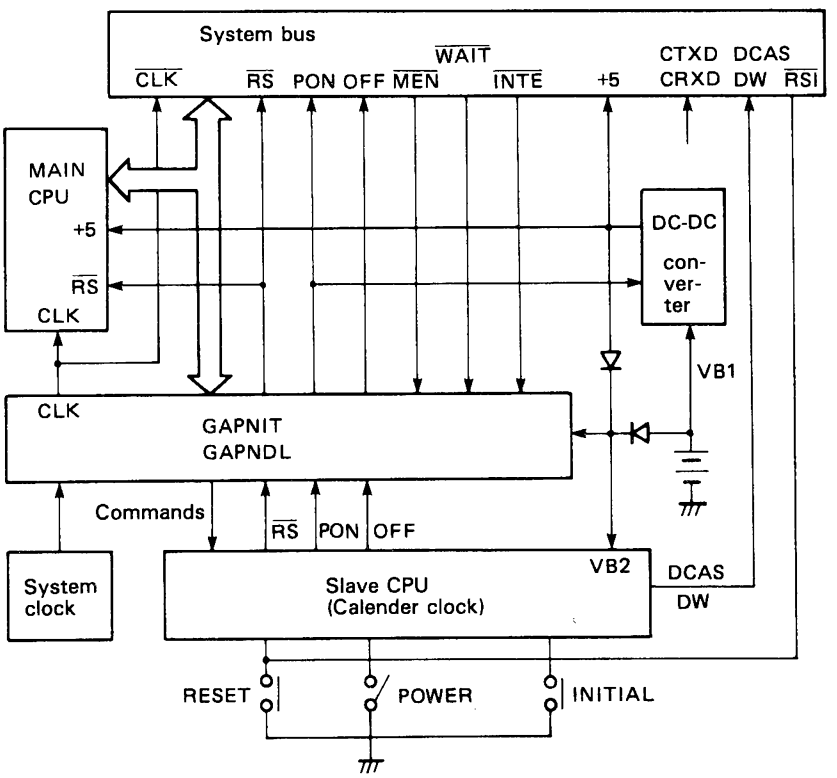
An optional external RAM disk can be connected to the system bus. Of the system bus signals, those which do not concern the Z-80 are used with the external RAM disk.

Included in the PINE's circuits are LSIs which operate on battery power even when the main power is turned off. The input terminals of two of these LSIs, GAPNDL and GAPNIT, are connected to the data bus and the address bus.

Other parts of the circuit control the power supply (+5V) to the main CPU, ROM, and the system bus. When the slave CPU detects the power switch signal or an alarm signal, it outputs the PON signal, starting the DC-DC converter and turning on the power. Once the power has been turned ON, it stays on until the main CPU commands the slave CPU to turn it off. Accordingly, the power can be turned off from within an application program.

Take note of the following points when using the system bus.

- o To avoid power supply problems, it is preferable that power to any user device connected to the system bus be supplied from the computer.
- o System bus signals are output directly from the main CPU. Therefore, errors may result if they are output to an external device through a cable.
- o Some of the system bus output signals are backed up by battery.
- o Use CMOS ICs in any circuit which is to be connected to the system bus. Incorrect operation will result if TTL compatible ICs are connected to the data or address bus, or if signal line levels are pulled up through resistors.



2.2.1 Main CPU (μPD70008C)

The CMOS Z-80 used as the PINE's main CPU differs from NMOS devices in the following respects.

- o The CPU goes into the standby mode when the HALT instruction is executed.
- o In the standby mode, no external operations (including memory refresh operation) take place. This reduces CPU current consumption. Output levels in the standby mode are as follows.

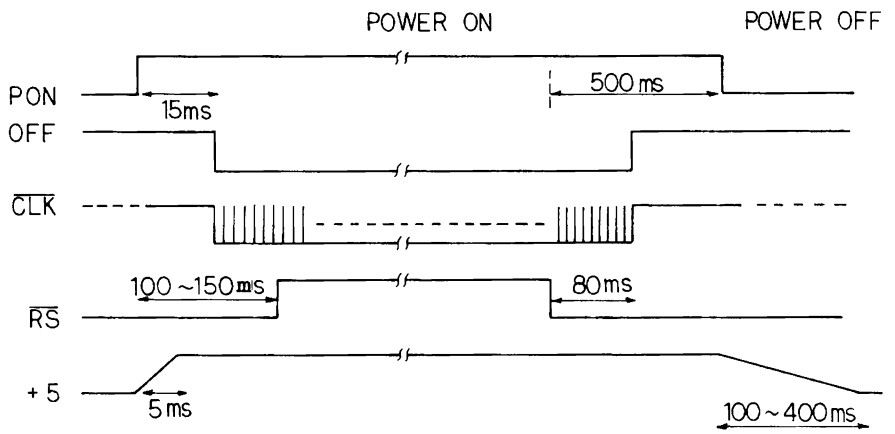
DB0 - DB7	HIGH or LOW
AB0 - AB15	HIGH or LOW
$\overline{\text{HALTA}}$	LOW
Other signals	HIGH

- o standby mode is reset by the RESET signal or the INT signal.
- o Load capacity is 100 pF.
- o Other

  The number of machine cycle states is greater due to factors involving memory access time. When an application program is executed in RAM, a WAIT state is added to M1 cycles so that there are five states. When the external RAM disk is accessed, 1 WAIT state is added.

Main CPU operation is not backed up by battery. Therefore, care should be taken when a user circuit is powered by batteries or any other external power supply.

The power ON/OFF sequence is as shown below.



2.2.2 ROM

With the PINE, CMOS ROMs are used in ROM capsules. Although it is possible to use NMOS ROMs for programs which are loaded for execution, they are not practical due to their large current consumption; in some cases, the DC-DC converter may lack sufficient capacity to supply such devices. Also, since power is supplied to ROM even when it is not being accessed, use of NMOS devices will result in much shorter battery discharge time.

ROM capsules may contain either 8KB, 16KB, or 32KB ROMs. Jumper plug settings should be changed as follows when using 16KB ROMs.

DRIVE: B	J5A - ON, J5B - OFF
DRIVE: C	J4A - ON, J4B - OFF

2.2.3 RAM

A 64K byte DRAM is used as the PINE's main memory. The contents of main memory are backed up by battery even when the power is turned off, and memory is self-refreshing. When the power is turned off, memory backup draws about Ø.6 mA from the batteries. When the power is on, GAPNDL--not the main CPU--controls DRAM memory refresh operation.

2.2.4 Slave CPU (75Ø8)

The slave CPU has its own built-in operating system, and performs the following functions.

- o Power ON/OFF and reset signal output.
- o Calendar clock control.
- o DRAM self-refresh mode control.
- o Keyboard control

The slave CPU runs on battery power even when the power is turned off and signal output to the system bus is maintained.

2.2.5 Custom LSIs

Three custom LSIs are used in the PINE. These LSIs are connected to the system bus.

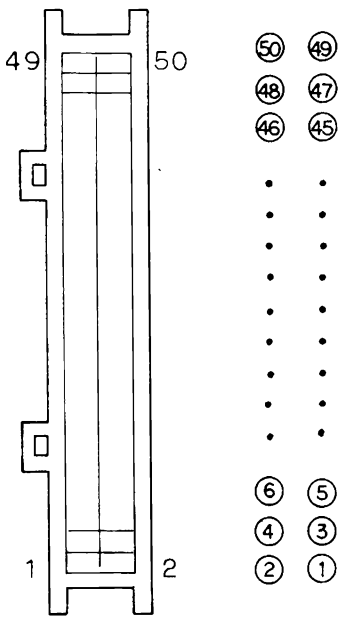
Other LSIs than GAPNIO maintain the states of registers while the power source are turned off to allow program execution to be resumed in the continue mode.
Although main CPU operation is stopped by the RS signal, operation of the custom LSIs is stopped by the OFF signal; this prevents them from being affected by external signals. Nevertheless, it is important that power to the LSIs be turned off when they are not operating. The reason for this is that excess power consumption results when CMOS gates are operated in a linear configuration.

2.2.6 Names and Functions of System Bus Connector Pins

PON	This signal turns on the DC-DC converter, and is output by the slave CPU. The signal is backed up by battery.
OFF	This signal becomes H when the power is OFF. When the signal drops back to L, power switches back to the ON state from the memory backup state. The signal is controlled by the slave CPU, and is backed up by battery.
CLK	The 3.6864 MHz system clock signal.
RS	The system reset signal. This signal is backed up by battery.
RSI	Setting this signal to L outputs a reset signal to the main CPU.
DCAS	This signal sets the self-refresh mode, and is required to use DRAM through the system bus. This signal is backed up by battery.
DW	Same as above.
MEN	When this signal is L, the main CPU accesses ROM or RAM in main memory. When this signal is set to H through the system bus, the main CPU accesses ROM or RAM belonging to the system bus. At such time, main memory RAM is refreshed and the main CPU can use the I/O registers in the usual manner.
WAIT	WAIT signal which can be input from the system bus.
INTE	Interrupt signal which can be input from the system bus. Ordinarily, such input is inhibited by the system program. This signal is backed up by battery.
CTXD	Serial data send line. This is connected to the ART through the cartridge interface. When used, the J2 jumper plug must be set on J2B.
CRXD	Serial data receive line. To use this signal, the J3 jumper plug must be set on J3B.

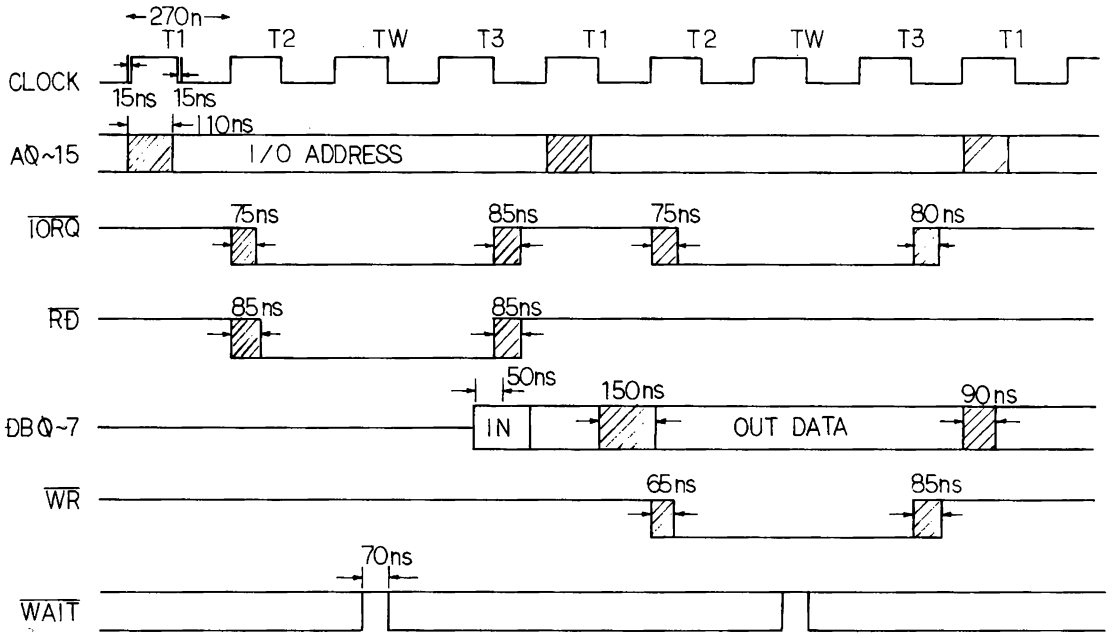
This manual does not explain the Z-80 input/output signals.

Connector HU-500S2D-L13T

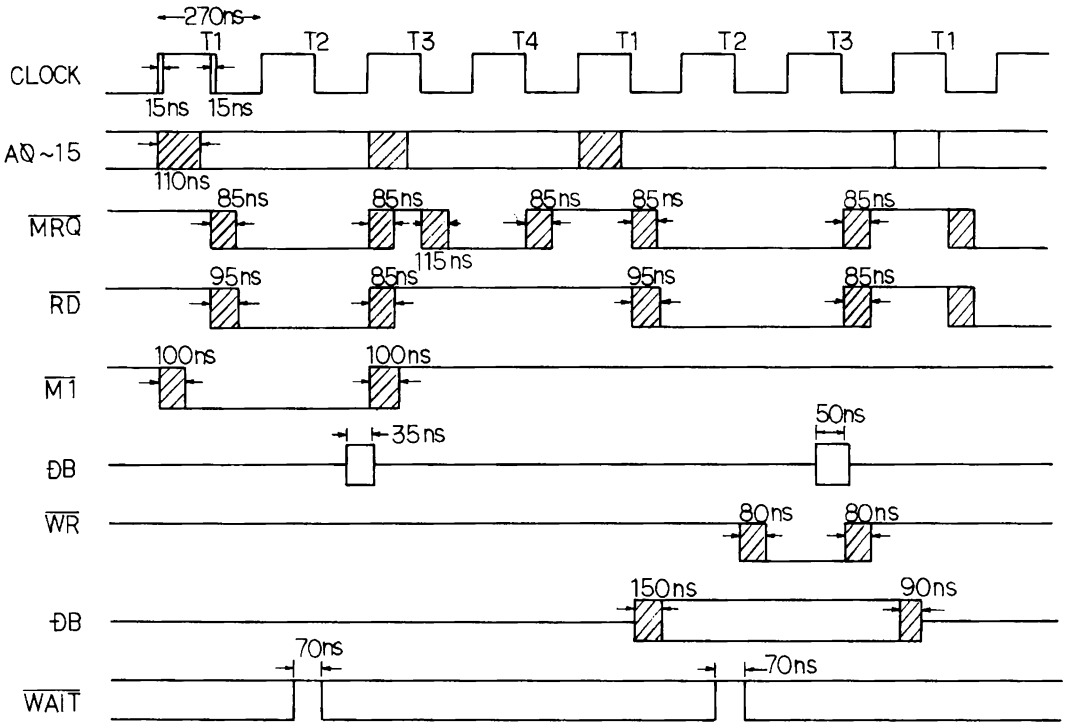


DCAS	49	50	RSI
OFF	47	48	DW
AB14	45	46	AB15
AB12	43	44	AB13
AB10	41	42	AB11
AB8	39	40	AB9
AB6	37	38	AB7
AB4	35	36	AB5
AB2	33	34	AB3
AB0	31	32	AB1
$\overline{RS}$	29	30	$\overline{M1}$
CG	27	28	CG
$\overline{HLTA}$	25	26	CRXD
$\overline{WR}$	23	24	$\overline{MRQ}$
$\overline{RD}$	21	22	$\overline{IORQ}$
$\overline{CLK}$	19	20	CTXD
$\overline{WAIT}$	17	18	PON
$\overline{MEN}$	15	16	$\overline{INTE}$
DB1	13	14	DB0
DB3	11	12	DB2
DB5	9	10	DB4
DB7	7	8	DB6
GND	5	6	VL(+5)
VB2	3	4	VBK
VCH	1	2	VB1

2.2.7 Input/Output Characteristics

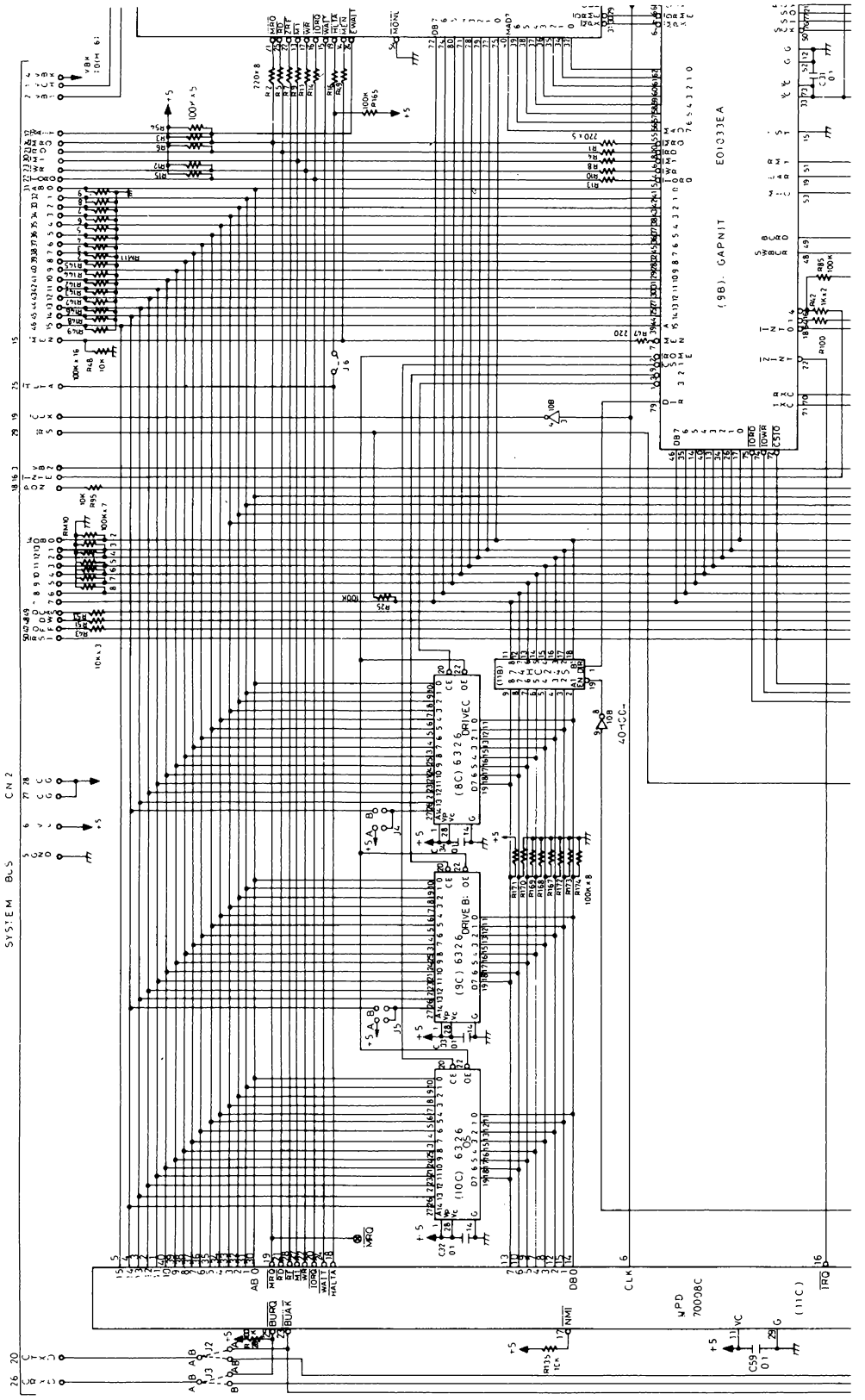


I/O READ/WRITE (SYSTEM BUS)

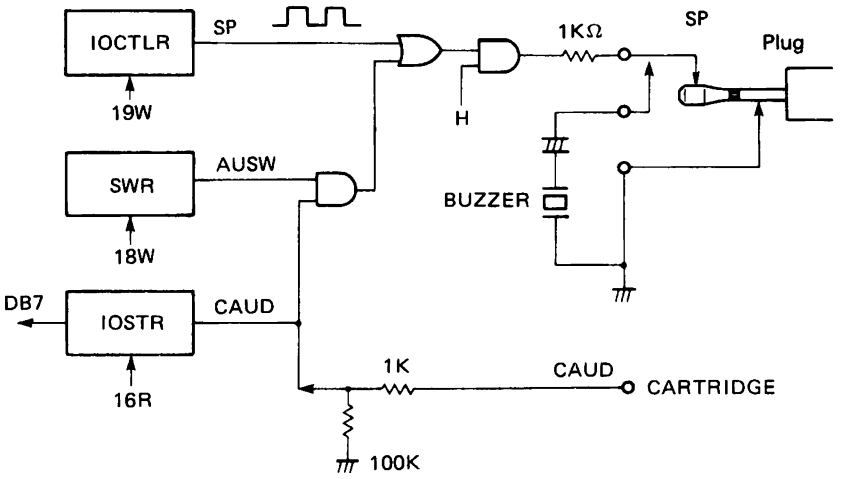


MEMORY READ/WRITE (SYSTEM BUS)

2.2.8 System Bus Circuit



2.3 Speaker Interface



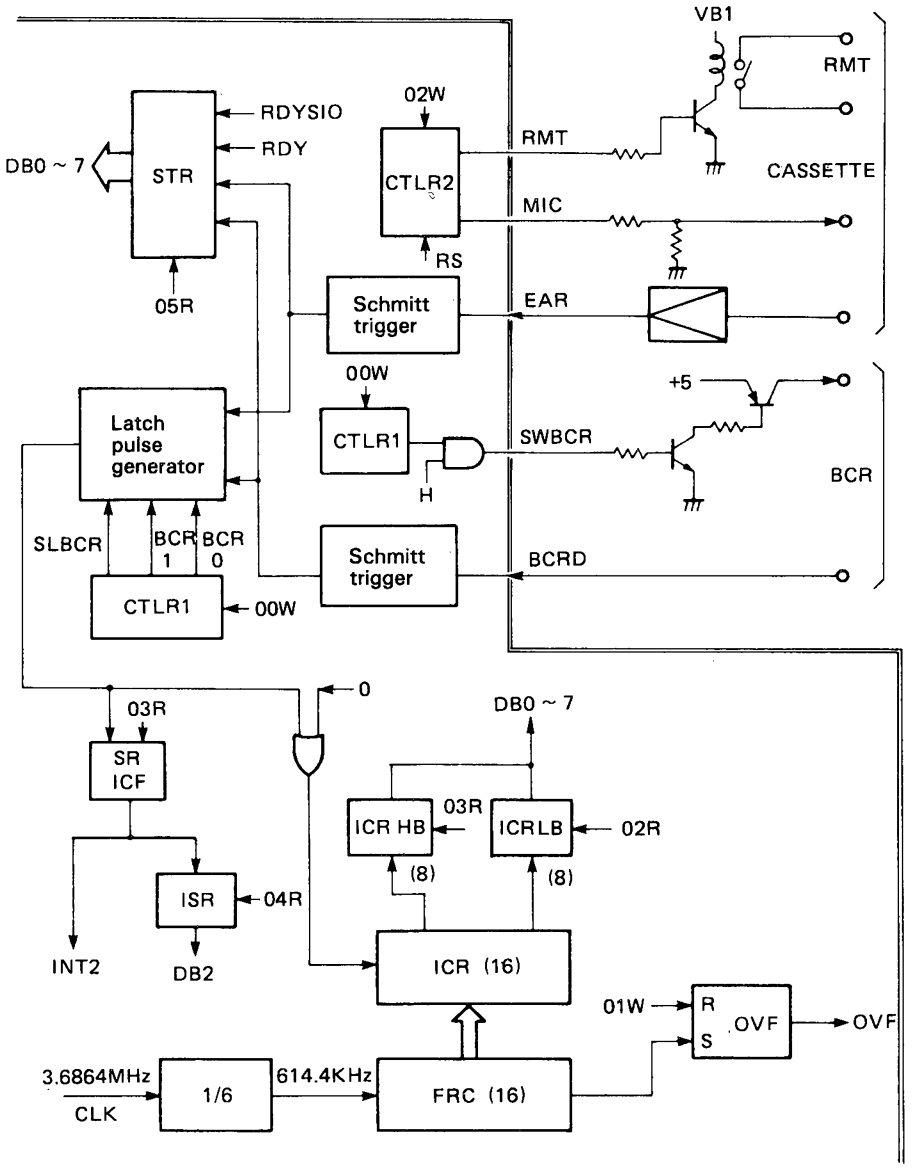
The PINE's speaker interface makes it possible to connect an external speaker or amplifier. The SP signal is switched for external output by inserting a plug into the speaker jack.

The SP signal is output by IOCTLR, but can also be input from pin CAUD of the cartridge interface.

The PINE's operating system manages the setting of the AUSW flag, which makes it possible to monitor microcassette drive output data through the speaker.

The volume of the PINE's built-in buzzer cannot be adjusted. Therefore, it the volume is not sufficient for use as an audible alarm, use an amplifier connected to the external speaker interface.

2.4 Bar Code Reader Interface



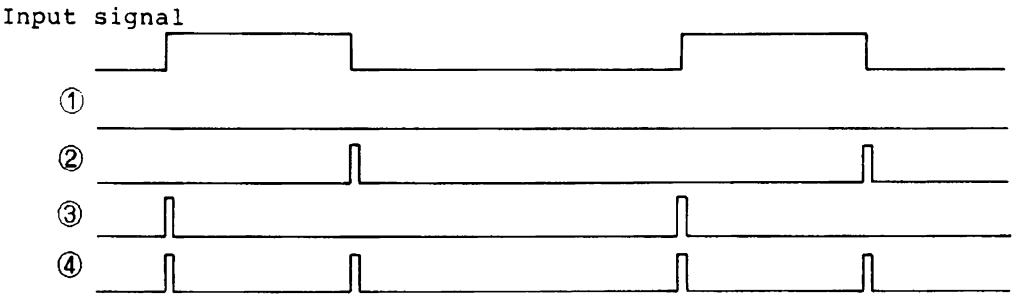
2.4.1 I/O Registers

The bar code reader interface makes it possible to measure the pulse width, pulse spacing, and frequency of signals input to the PINE. The signal input to BCR can be read by the main CPU using status register STR. Likewise, the value of the free running counter (FRC) is latched into latched in input capture register ICR each time the signal level changes; this makes it possible to measure the interval between one latch pulse and the next.

Latch pulse generation can be detected through the input capture flag (ICF). The ICF is reset whenever ICRHB is accessed.

The ICF can be used to generate interrupts, but since a relatively great amount of time is required for processing it is preferable to use the input status register (ISR).

The method used for latch pulse generation can be selected as shown below by changing the setting of control register CTL1.



Flag settings are determined as follows for each type of latch pulse generation.

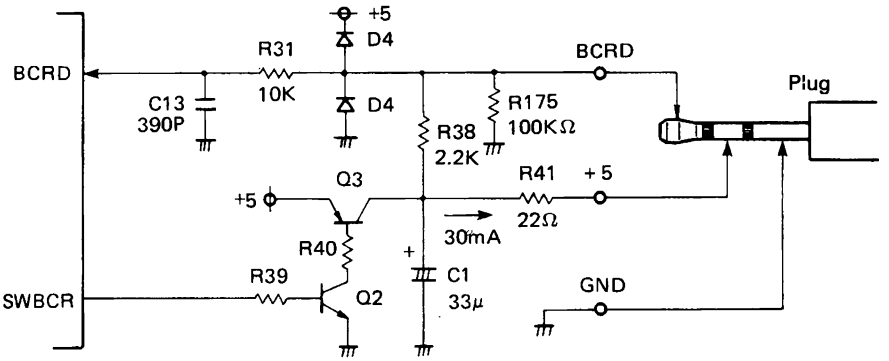
	BRG3	-	BRGØ		SWBCR	BCR1	BCRØ	SLBCR
(1)	Ø	1	1	Ø	Ø	Ø	Ø	Ø
(2)	*	*	*	*	Ø	Ø	1	1
(3)	*	*	*	*	Ø	1	Ø	1
(4)	*	*	*	*	Ø	1	1	1

Settings indicated by asterisks are determined from the contents of memory address FØØ1H.

Method (1) is the operating system's initial setting. Use method (2) or (3) when measuring pulse interval or frequency, and use method (4) (together with STR) when measuring pulse width or interval. Method (4) is the one used with the bar code reader.

The FRC (a 16-bit counter) counts pulses produced by dividing the system clock; these pulses have an interval of about 1.6 μsec. Therefore, time differences of up to about 1Ø6 ms can be measured. Greater intervals can be measured by checking the OVF flag.

2.4.2 Bar Code Interface Circuit



Power can be supplied to a device connected to the BCR jack by setting the SWBCR flag. This is shown in the figure above.

Signals input at the BCRD terminal are integrated by C13 and R31. Thus, the maximum frequency which can be measured through the interface is from 40 to 100 kHz.

Diode D4 provides input terminal protection. When the input voltage exceeds +5V or an alternating current signal is input, be sure to connect a resistor in series with the signal line to limit current.

2.4.3 Sample Program

The following program illustrates use of the bar code reader interface to measure signal frequency. This program can be used to measure signal frequencies in the range from 10 to 50 Hz.

```
 10  OUT &H00, &H65
 20  ICR=INP(&H03)
 30  ISR=INP(&H04)
 40  F=ISR AND &H04
 50  IF F=0 GOTO 30
 60  ICR1=INP(&H02):ICR2=INP(&H03)
 70  ISR=INP(&H04)
 80  F=ISR AND &H04
 90  IF F=0 GOTO 70
100  ICR3=INP(&H02):ICR4=INP(&H03)
110  T1=256*ICR2+ICR1
120  T2=256*ICR4+ICR3
130  T=T2-T1
140  IF T>0 THEN T=T ELSE T=T+65536!
150  LOCATE 1,1
160  F=1000/(T*(1/614.1))
170  PRINT F; "HZ"
180  GOTO 10
190  END
```

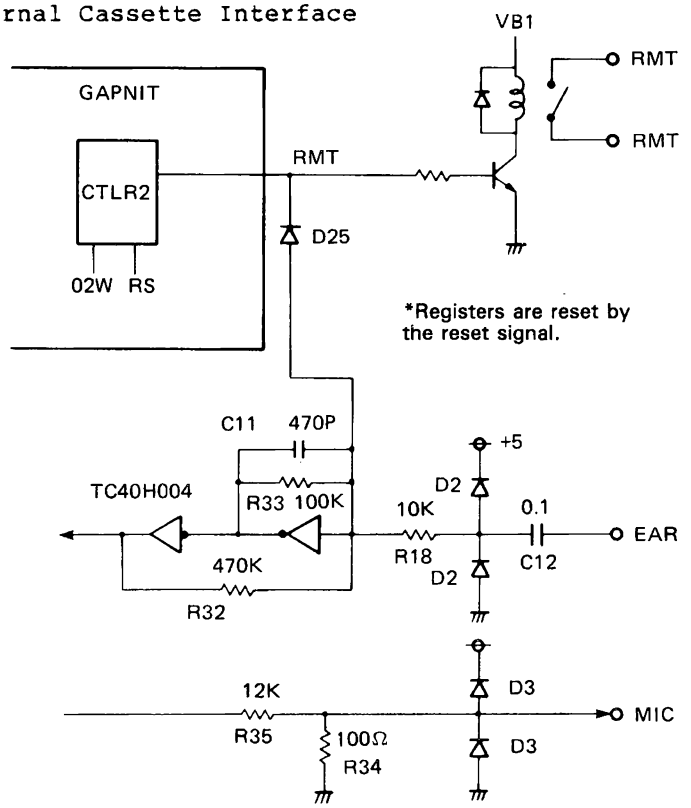
Since the above program is not of practical use, it can be improved by changing the part which measures time (lines 20 to 130) to machine code as follows.

```
 10   FORI=0 TO 34
 20   READ A:POKE &H6000+I, A
 30   NEXT
 40   DATA &HE5, &HDB, &H03, &HDB, &H04, &HE6,
           &H04, &H28, &HFA, &HDB, &H02, &H5F,
           &HDB, &H03, &H57, &HDB, &H04, &HE6,
           &H04, &H28, &HFA, &HDB, &H02, &H6F,
           &HDB, &H03, &H67, &HED, &H52, &HEB,
           &HE1, &H73, &H23, &H72, &HC9
100   OUT &H00, &H65:CLS
110   DEF USR1=&H6000
120   T%=USR1(0)
130   IF T%>0 THEN T=T% ELSE T=T%+65536!
140   F=1000/(T*(1/614.1))
150   LOCATE 1,1
160   PRINT USING "#####.#";F;
170   PRINT"  HZ":FOR I=0 TO 500:NEXT
180   GOTO 120
190   END
```

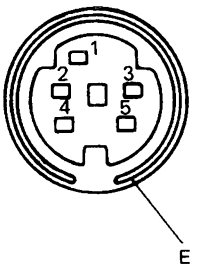
This program can measure signal frequencies in the range from 10 Hz to 20 kHz. Since the minimum unit of time measurement is 1.6 μsec, error increases when measuring signal frequencies above 20 kHz.

Note that the bar code reader interface, timer circuit, and external cassette interface cannot be used at the same time.

2.5 External Cassette Interface



Connector



Pin NO.	Symbol
1	GND
2	RMT
3	RMT
4	MIC
5	EAR
E	–

Plug TCP8050-01-020

The external cassette interface uses the same circuit as the bar code reader interface. See the explanation of the bar code reader interface for details.

When using this interface, set the SLBCR flag to Ø. This makes it possible to generate latch pulses when signals are input from the cassette connector.

Also be sure to set the RMT flag.

The signal input from the EAR terminal is amplified by a CMOS linear amplifier to about 1Ø times its original level, then the signal waveform is shaped by a Schmitt circuit. This circuit has a narrow frequency range, and only amplifies signals in the range from 1 to 2 kHz. The signal output to the MIC terminal has a voltage level of about 4Ø mVpp.

The remote output relay contacts cannot be used to turn a 1ØØ VAC load ON or OFF directly. The load should not be greater than about 24V, Ø.5 A.

2.6 Serial Interface

The ART (asynchronous receiver/transmitter) used in the PINE's serial interface is equivalent to the 8251. However, the device only provides those 8251 functions which are required for use with the PINE.
The transmitter and receiver are completely independent, and each of them inputs a separate clock from the baud rate generator.

The transmitter and receiver use a double buffer structure. Therefore, when using XON/XOFF control, even after the PINE receives the XOFF character during output, it may output 2 or 3 bytes of data before halting.

In addition to the buffer built into the 8251, 240 bytes of main memory are used as a receive buffer.

When the ART receives data, it outputs interrupt signal RRDY to the main CPU.

By changing the setting of switch register SWR, the serial interface's ART can be used from any of the following connectors.

RS-232C	Input, ±15V; output, ±5V
Serial	Input, ±15V; output, ±5V
Cartridge interface	Logic circuit levels
System bus	Logic circuit levels

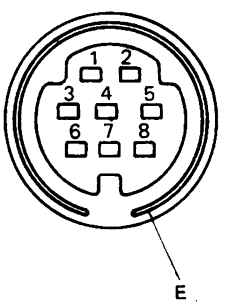
The serial connector provides only RS-232C modem interface signal lines, but the circuit configuration of the driver/receiver is the same as with the RS-232C connector.

With the PINE, a CMOS IC is used for the driver/receiver. Because of this, significant waveform deterioration due to interline capacitance will result if a long interface cable is connected. This means that lower transfer rates may be required with longer interface cables.

The RS-232C cable may be up to 10 to 20 meters long. The maximum usable length will vary according to the structure of the cable and the manner in which it is installed.

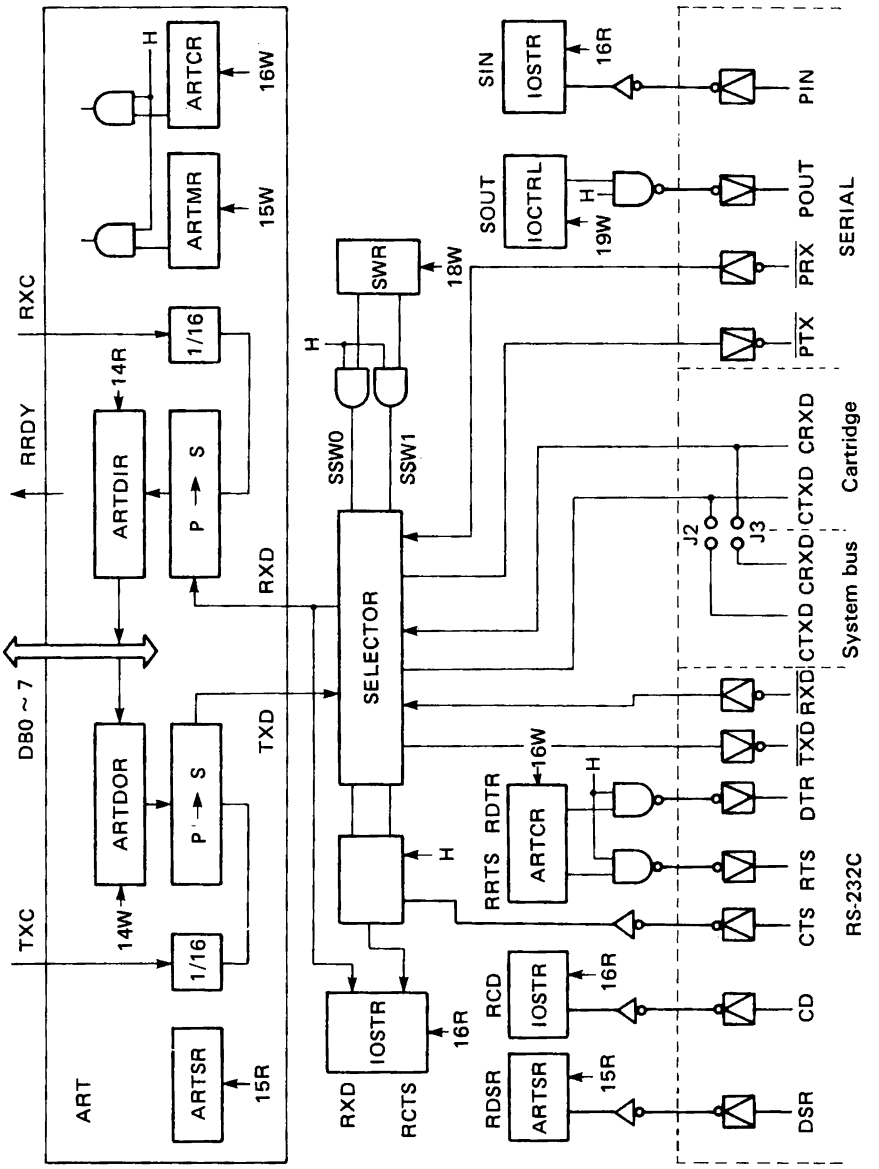
The levels of the RTS, DTR, and POUT lines are automatically set to H when BASIC is started. If this causes inconvenience, they can be returned to the L level by opening the interface for communication, then closing it again.

Connector

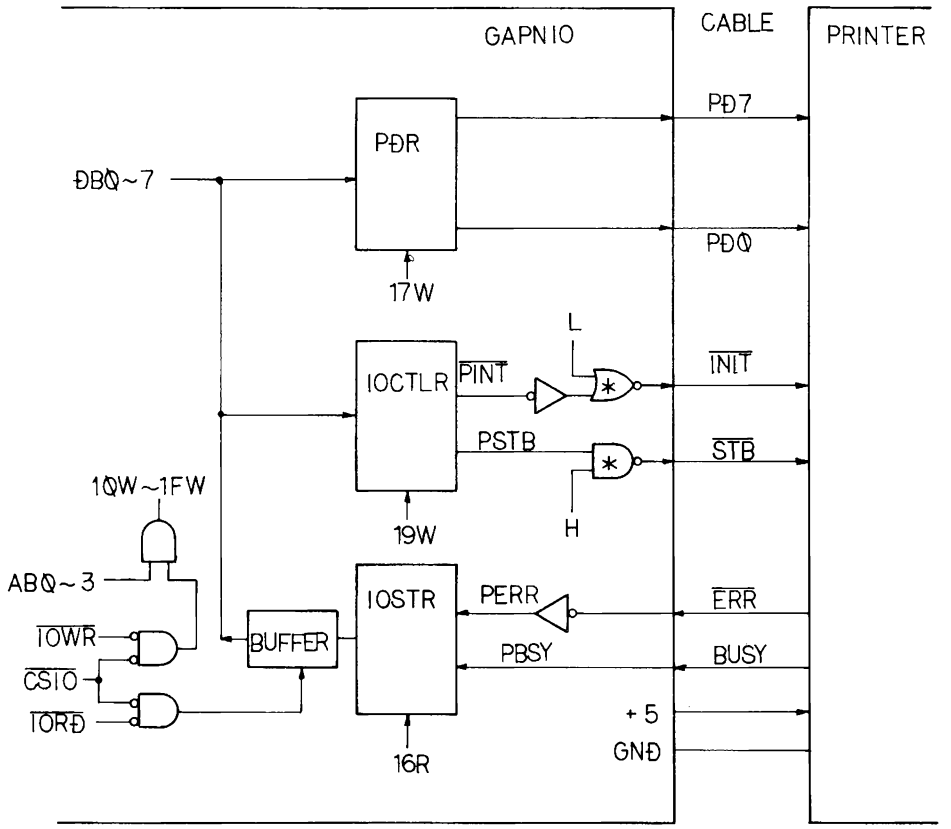


	RS-232C	Serial
Pin No.	Symbol	Symbol
1	GND	GND
2	TXD	PTX
3	RXD	PRX
4	RTS	
5	CTS	
6	DSR	PIN
7	DTR	POUT
8	DCD	
E	CGND	CGND

Plug TCP8080-01-020


ART
ARTSR
15R
ARTDOR
14W
ARTDIR
14R
ARTMR
15W
ARTCR
16W
1/16
P → S
TXC
RXC
RRDY
DB0 ~ 7
TXD
RXD
SELECTOR
SSW0
SSW1
SWR
18W
IOSTR
16R
RXD
RCTS
RDSR
RCD
RRTS
RDTR
SOUT
IOCTRL
19W
SIN
DSR
CD
CTS
RTS
DTR
TXD
RXD
PIN
POUT
PRX
PTX
SERIAL
RS-232C
J2
J3
CTXD
CRXD
System bus
Cartridge

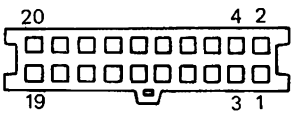
2.7 Printer Interface



*Registers are reset by the reset signal

Connector: HU-200P2 (DDK)

CG	2	1	CG
BSY	4	3	PD7
+5	6	5	PD6
+5	8	7	PD5
GND	10	9	PD4
$\overline{ERR}$	12	11	PD3
GND	14	13	PD2
$\overline{INIT}$	16	15	PD1
GND	18	17	PD0
NC	20	19	$\overline{STB}$



When no LIST device is connected to the printer interface, it can be used for purposes other than printing.

A TTL compatible IC can be connected to the interface, and all outputs can be used to drive LEDs. When doing this, the LEDs should be connected to GND through a 1K ohm resistance. However, no more than one of these LEDs should be lit at any given time.

Input/output specifications of custom LSIs used with the PINE are as follows.

Output voltage	VOH	3.7 V min.	IOH = -Ø.4 mA
	VOL	Ø.4 V max.	IOL = 2 mA
Input voltage	VIH	2.6 V min.	
	VIL	Ø.7 V max.	

Output terminal capacitance:	8 pF max.
Input terminal capacitance:	8 pF max.
Input/output terminal capacitance:	12 pF max.

Chapter 3 Sample Programs

This chapter presents some sample programs which may be useful as reference when preparing application programs in BASIC.

3.1 Printer Interface

The following program gives an example of use of the printer interface. The status of the I/O control register is determined from memory address F006H.

```
10 OUT &H17,&HFF
20 OUT &H17,&H00
30 OUT &H19,&H02
40 OUT &H19,&H01
50 PRINT HEX$(INP(&H16))
60 GOTO 10
```

This program sends a pulse signal to the output port, then reads and displays the status of the input port.

Upon running this program, "4A" is displayed.

3.2 1-Second Counter

The 1-second counters are located in the memory area which is used by the calendar clock for counting 1-second signals. These signals are counted by the operating system, and the counters can be set and used for any purpose desired. Ordinarily, they are used for controlling auto power-off operation. The location of the counters and a sample program which displays the value of one of them are shown below.

```
EF90   EF8F   - Upward count
EF92   EF91   - Downward count
```

```
10 A=PEEK(&HEF91)
20 B=PEEK(&HEF92)
30 PRINT B*256+A
40 GOTO 10
```

3.3 1/10-Second Counter

This is a 16-bit timer counter which generates an interrupt upon decrementing from FFFFH to 0000H. Since the interrupt is generated at 106.667 ms intervals, it can be used as a count lock.

Whether or not an interrupt has been generated can be determined by monitoring the interrupt flag at address EFD3H. This flag should be reset after it has been read.
The contents of the flag byte and a program which reads and resets it are shown below.

```
EFD3H  Bit 7  7508
           6  ART
           5   /
           4  ICF
           3  OVF   Timer counter OVF
           2  EXT
           1   /
           0   /
```

```
10 A=PEEK(&HEFD3)
20 B=A AND &H08
30 IF B=0 GOTO 10
40 POKE &HEFD3,&H00
50 C=C+1
60 PRINT C*(65.563/614.4)
70 GOTO 10
```

3.4 DIP Switch

The function of DIP switch SW7 (where DIP switch bit 0 is SW1) can be defined for use by the user. The status of this switch is determined by reading memory address F775H. A "1" at this address indicates that this switch is ON; a "0" indicates that it is OFF. However, if the switch setting is changed, the contents of F775H do not change until the system is reset.

```
10 D=PEEK (&HF775)
20 S=D AND &H40
30 PRINT HEX$(S)
40 END
```

3.5 LEDs

The status of the I/O control register can be determined by referencing memory address F006H as shown in the example below.

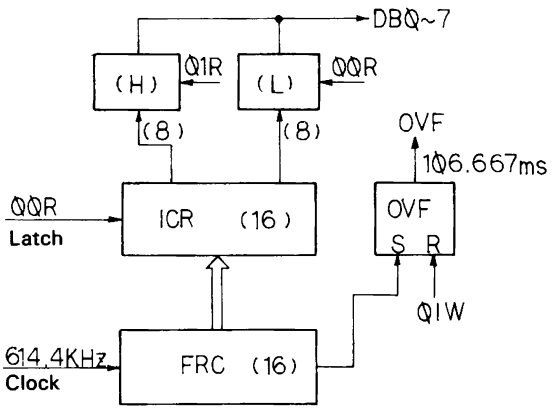
```
LED ON
10 IO=PEEK(&HF006)
20 LED=IO OR &H40
30 POKE &HF006,LED
40 OUT &H19,LED
50 END

LED OFF
10 IO=PEEK(&HF006)
20 LED=IO AND &HBF
30 POKE &HF006,LED
40 OUT &H19,LED
50 GOTO 10
```

3.6 Remote Output

Relay ON: OUT 2,2
Relay OFF: OUT 2,0

3.7 Timer

Timer Circuit



With the PINE, elapsed time is determined by latching the free running counter value in the input capture register. The FRC is continuously incremented by the system clock and the OVF flag is set to generate a main CPU interrupt when the counter overflows. The OVF flag is reset by the operating system.

The FRC value can be latched in the ICR by reading address 00H; this causes the main CPU to read the lower 8 bits of the counter.

Note that the timer cannot be used simultaneously with an external cassette recorder or bar code reader because these preempt use of the timer circuit.

The following program measures execution time of the OUT statement (about 2 ms).

```
10 C=INP(&H00) : D=INP(&H01)
20 OUT 2,2
30 A=INP(&H00) : B=INP(&H01)
40 F=256*D+C
50 S=256*B+A
60 T=S-F : IF T<=0 GOTO 70 ELSE 80
70 T=T+65536
80 PRINT T*(1/614.4)-5.7 : '(ms)
90 END
```

3.8 Power ON

The PINE's wake function makes it possible to have the computer turn itself on and execute a program even when the power switch is in the OFF position. This function is particularly useful in applications requiring automatic metering or schedule management.

The wake function is controlled using the calendar clock even when the power is off; upon reaching a preset time, the function automatically turns on the power. The wake time can be set either from the SYSTEM DISPLAY or with the ALARM statement.

If the program ends by turning the power off in the continue mode, program execution can be automatically resumed each time the power goes back on.

When using the following program, use all asterisks when setting the wake time; this causes the power to go on at 1-minute intervals.

The following program outputs the date and time to the printer.

```
10 LPRINT DATE$;"***";TIME$
20 FOR I=1 TO 2000:NEXT
30 POWER OFF,RESUME
40 GOTO 10
50 END
```

The purpose of the FOR-NEXT loop on line 20 of this program is to allow time for printing to finish before turning off the power. This is necessary whenever data is output to the printer.

The following program saves the time to RAM disk.

```
10 OPEN "O",#1,"A:TEST.DAT"
20 T$=TIME$
30 IF T$>"20:00:00" THEN 70
40 PRINT#1,T$
50 POWER OFF, RESUME
60 GOTO 20
70 CLOSE
80 END

100 OPEN "I",#1,"A:TEST.DAT"
110 IF EOF(1) THEN 140
120 INPUT#1,A$:PRINT A$
130 GOTO 110
140 END
```

3.9 Power OFF

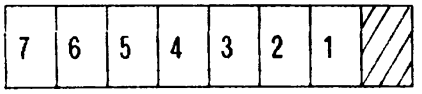
This section explains how to use user interfaces with the continue mode.

The PINE's operating system cannot operate user-designed circuits in the continue mode. Therefore, processing involving such circuits must be done within an application program.

Procedure

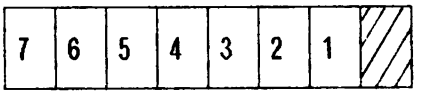
1. Set bit Ø of the power OFF inhibit flag to Ø to allow the power to be turned off from within the application program.

YPOFDS bit (EFEFH)



2. Check the power OFF status flag from with a program loop.

YPOFST bit (EFFØH)



These flags are set when a power OFF interrupt occurs, so following this, processing required for the continue mode is carried out.

3. Reset bit Ø of the status flag byte.

4. Do continue mode processing.

   o Set the continue mode flag.
   o Save any needed data.

5. Verify that no other status flags are set, then execute POWER OFF,RESUME.

6. When the power goes back on, check the continue mode flag and do the following processing.

   o Set register modes, load data, etc.
   o Reset the continue mode flag.

If there are any keyboard input statements in the program loop, the power is turned off by the operating system in the non-continue mode. Therefore, use INKEY$ when keyboard input is required.

The power OFF inhibit flag can be reset interrupting program execution and turning off the power switch.

```
 10 IF F=0 GOTO 40 ELSE 20
 20 SOUND 100,100
 30 F=0
 40 A=PEEK(&HEFEF)
 50 A=A OR &H01
 60 POKE &HEFEF,A
 70 C=C+1:PRINT C
 80 B=PEEK(&HEFF0)
 90 IF B=0 GOTO 70 ELSE 100
100 B=PEEK(&HEFF0)
110 B=B AND &HFE
120 POKE &HEFF0,B
130 SOUND 300,100
140 F=1
150 POWER OFF,RESUME
160 GOTO 10
```

Chapter 4 Power Supply

Chapter 4 - Power Supply

4.1 Outline

This chapter discusses the PINE's power supply.

The PINE is powered by a replaceable main battery and a rechargeable sub-battery which is built right into the computer. When the power is ON, the logic circuit power supply is obtained from the main battery through a DC-DC converter. When the power is OFF, current for memory backup is provided by the main battery and the sub-battery.

The power is turned ON and OFF by commands, and DC-DC converter operation is controlled by a signal called PON. Power supplies to the various interfaces are shown in the block diagram given later in this chapter.

The +5 V power supply can supply 60 to 100 mA to an external device connected to the computer. This capacity is reduced as indicated below when the following optional devices are used.

Microcassette drive	25 mA
Bar code reader	35 mA
Other	3 mA

If the DC-DC converter is overloaded, a drop in output voltage will result.

VB2 is the power supply for memory backup. When the power is ON, this is supplied by the DC-DC converter; when it is OFF, it is supplied by the batteries.

VB1 is a non-regulated power supply which powers operation of various devices. GB is the grounded side of VB1.

VCH is the charging power for the NiCd battery.

The PINE can be used with a special AC adapter for EPSON handheld computers. Connect the adapter to the AC adapter jack to use an external power supply. Although the computer will operate on voltages as low as 6V, 8 to 9 V is required in order to charge the built-in battery.

The AC adapter output goes into a regulated power supply. Therefore, damage to the computer may result if the input voltage is excessively high.

When using the AC adapter, the NiCd batteries are charged regardless of whether the power is ON or OFF. As long as the power supply voltage is in the range from 7.5 to 8V, the NiCd batteries are capable of at least one year of continuous operation even if overcharging occurs.

If battery voltage drops below 4.8V, a power failure is detected and the "CHARGE BATTERY" message is displayed. Unless the batteries are then charged, the contents of memory will be lost. However, this does not occur immediately, but only after some time has past.

If the contents of memory are lost, operation begins with display of the system initialization screen once the power is restored.

Battery capacity: Main batteries - 450 mAH
Charging current - 70 mA
Sub battery - 90 mAH
Charging current - 3 mA

Discharge current: When using a NiCd battery pack without connecting any optional devices

During BASIC program execution - 105 mA
While BASIC is waiting for key input - 65 mA

Discharge time:During BASIC program execution
NiCd batteries - 4.0 hours
Manganese batteries - 5.5 hours
Alkaline batteries - 11.5 hours

Memory backup time: With main+sub batteries - 900 to 1000 hours
With sub battery only - 150 hours

Memory backup current is about 0.6 mA at 25°C (77°F).

Power supply combinations

E	D	C	B	A	
O	O		O		AC adapter
			O	O	Manganese batteries
	O	O			NiCd batteries
O	O	O	O	O	Sub-battery

Power sources used with the PINE are manganese batteries, NiCd batteries, an AC adapter, and the built-in sub-battery.

1. Manganese batteries

When manganese batteries are used, continuous operation is possible even when the batteries are replaced. When the battery voltage drops below 4.0 V, the "CHARGE BATTERY" message is displayed and the batteries must be replaced. Memory is backed up by the sub-battery until replacement. Battery discharge can be avoided by using the AC adapter.

2. NiCd batteries

Up to 500 charge-discharge cycles are possible when using NiCd batteries. When the battery voltage drops below 4.8 V, the "CHARGE BATTERY" message is displayed and the batteries must be charged by plugging in the AC adapter. If the power switch is left in the OFF position at this time, charging is completed in 8 to 10 hours.

The batteries will be overcharged if the PINE is continuously operated with the AC adapter connected, but this will not result in any damage.

3. AC adapter

The PINE can be operated by connecting the AC adapter even when no main batteries are installed. When doing this, be sure to set the backup switch to the ON position.

The AC adapter used is rated at 6 V, 600 mA.

4. Sub-battery

The sub-battery is very important for assuring a stable supply of power to the computer's circuits.

When using the PINE, be sure to set the backup switch to the ON position. Damage to the computer may result if it is used with the AC adapter while the backup switch is set to OFF.

When the power is ON, the sub-battery is charged by the DC-DC converter. When the AC adapter is used, it is also charged while the power is OFF.

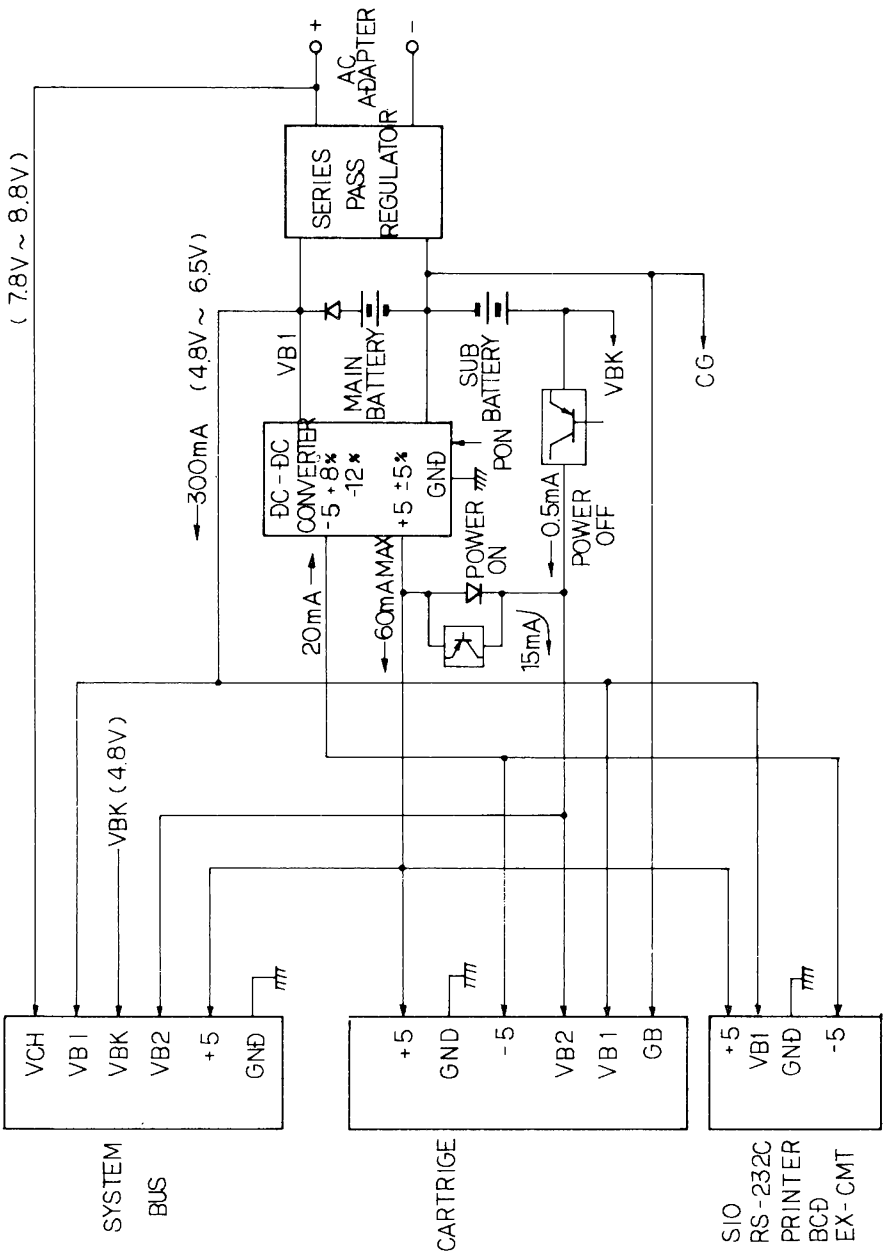
If the sub-battery becomes completely discharged, full charging requires about 45 hours.

Power failures

When the battery voltage drops below a certain point, the PINE detects a power failure. Current is supplied by the sub-battery while the main CPU is doing power failure processing. The sub-battery also automatically starts supplying current if a current surge causes the battery voltage to drop temporarily. In this case, a power failure is not detected.

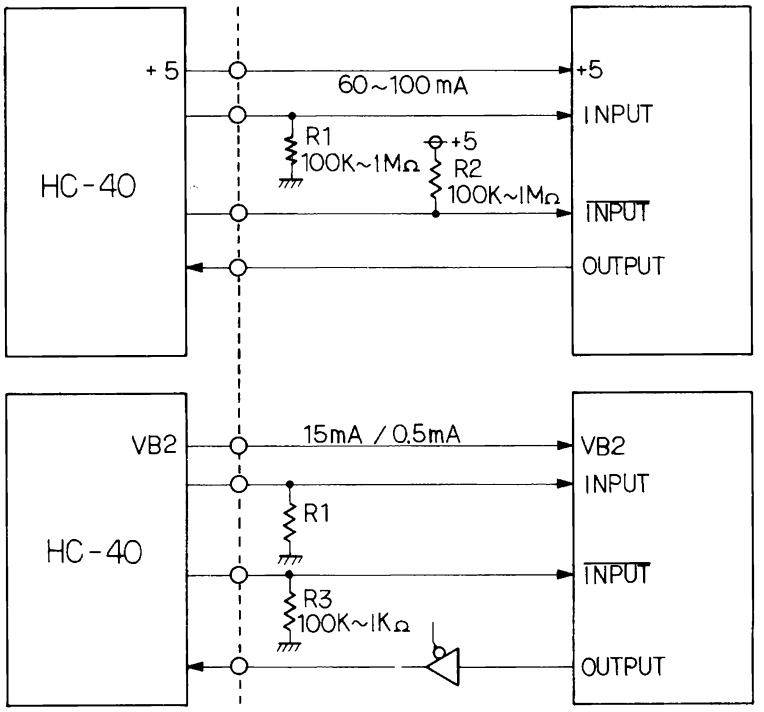
When the sub-battery condition is normal, the +5 V power supply is constantly regulated as long as the power is ON.

Note that power failures are not detected when power is supplied by the AC adapter or an external power supply.


(7.8V ~ 8.8V)
AC ADAPTER
+
-
SERIES PASS REGULATOR
VB1
MAIN BATTERY
SUB BATTERY
VBK
CG
300mA
(4.8V ~ 6.5V)
DC-DC CONVERTER
-5 +8%
-12 %
+5 ±5%
GND
PON
POWER ON
POWER OFF
0.5mA
20mA
60mA MAX
15mA
VBK (4.8V)
VCH
VB1
VBK
VB2
+5
GND
SYSTEM BUS
+5
GND
-5
VB2
VB1
GB
CARTRIGE
+5
VB1
GND
-5
SIO
RS-232C
PRINTER
BCD
EX-CMT

4.2 Pull-up and Pull-down

4.2.1 Cartridge Interface



External Circuit Example

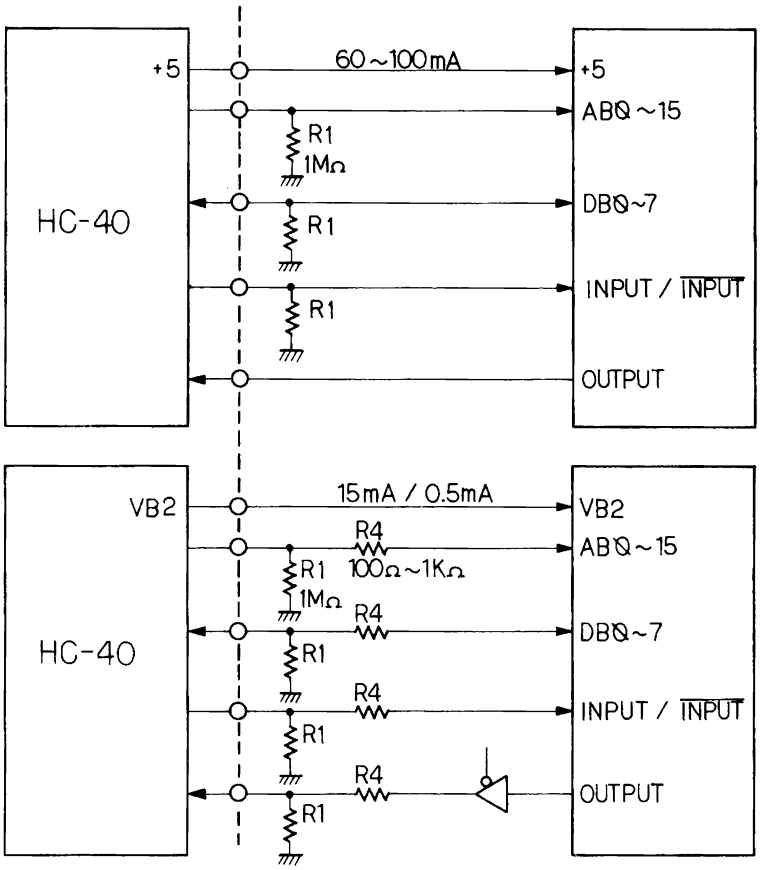
When power to an external circuit is supplied from the computer, the same method should be used to signal voltages up or down as is used within the computer itself.

When an external power source is used with an external circuit or battery backup is provided, the input signal should be pulled down. This prevents excess current from flowing into the computer from the external circuit when the computer power is turned off. For the same reason, tri-state output should be used for output signals to the external circuit.

In the circuit shown above, resistors R1 to R3 provide input terminal protection.

Note that no measures need be taken to prevent latch up with the cartridge interface.

4.2.2 System Bus



External Circuit Example

Be sure to observe the following rules when using the system bus.

- To protect input terminals, pull signal voltages down through a 1 megohm resistance.
- Do NOT pull up the address bus or data bus. If pull-up is required, do it at the RS line.
- If an external power supply is to be used with the external circuit (or external circuit operation is to be backed up by battery), insert resistance R4 to prevent latch-up.

Chapter 5 Notes Concerning Circuit Design

Chapter 5 - Notes Concerning Circuit Design

Observe the following precautions with regard to any external circuit which is to be connected to the PINE.

1. Operation of cartridge interface and system bus signals is assured only for circuits which can be connected directly to the PINE. Incorrect circuit operation may result if the circuit is connected through a cable.
2. If the circuit connected to the system bus is to be powered by an external power supply or backed up by battery, take the need to prevent latch-up into account when designing the circuit.
3. The standard length of the PINE's option cable is 1 meter. The computer's interface circuits are not designed to allow connection through a longer cable. Therefore, some type of buffer circuit is required if the external device is to be connected through a cable.
4. If computer signals are to be output through a cable, measures must be taken to protect against static electricity, external noise, and electromagnetic interference. Measures which are ordinarily taken are as follows.

   - o Shielding the cable.
   - o Using a cable of the minimum required length.
   - o Increasing the width (thickness) of the GND pattern and GND lines.
   - o Using a twisted pair cable and grounding one side.
   - o Passing signal I/O through a buffer circuit.
   - o Using photocouplers to separate physical circuit grounds.
   - o Whenever possible, using CMOS ICs and slow switching times (tf and tr).
   - o Operating circuits at low frequencies.
   - o Minimizing circuit impedances.
   - o Attaching a shield plate to the bottom of the external circuit's PCB and connecting this plate to chassis ground.

5. The RS-232C interface consists of a CMOS circuit, and no RS-232C line driver or receiver is used. Accordingly, operation is not assured if the cable used is longer than 10 to 20 meters.
6. Power to the external circuit may be supplied from the computer circuit. However, note that supply capacity is limited.
7. Use either CMOS or NMOS ICs in the external circuit. Also, note that TTL gates (IOL = 2.0 mA, IOH = -400 μA) can be connected to the printer interface.
8. When using a flat cable with the system bus, connect unused signal lines to ground through resistors on the external circuit side. Failure to do this may result in incorrect operation.
9. The system bus connector only has one GND terminal. Therefore, GND impedance can be reduced by connecting the GND line (pin 27) to the CG line (pin 28) on the external circuit side.