Data Systems

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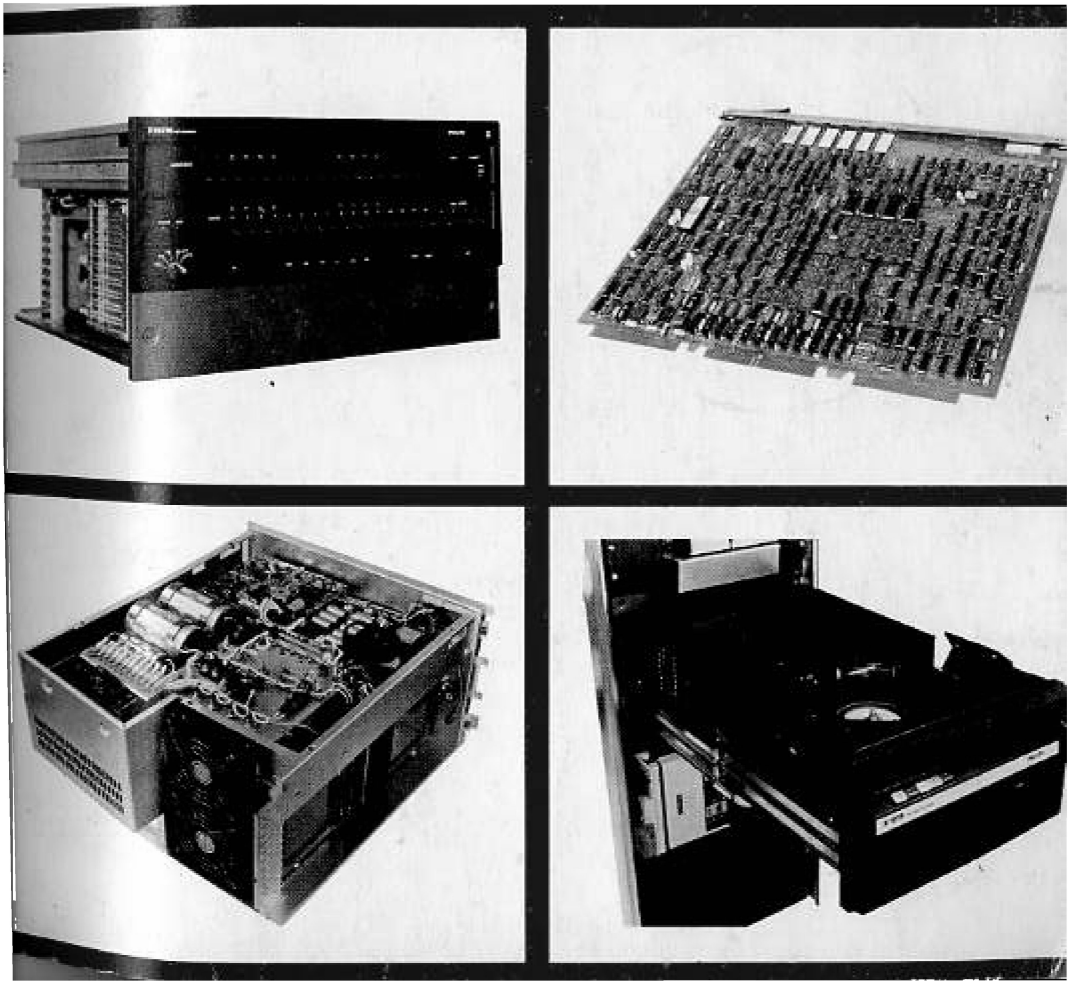
P856M/P857M System Handbook



- ASYNCHRONOUS GENERAL PURPOSE BUS
- SINGLE CARD MICROPROGRAMMED CPU
- INTEGRATED CONSOLE CONTROL UNIT
- CYCLE SPEED OF 1.2 OR 0.7 MICROSECONDS
- MEMORY MODULES OF 8 OR 16K WORDS
- MEMORY CYCLES INTERLEAVING
- MODULAR SYSTEM
- 16-BIT WORD ORIENTED
- 16 GENERAL PURPOSE REGISTERS
- MEMORY MANAGEMENT UNIT (P857M), 2K WORD PAGE SIZE
- FLOATING POINT PROCESSOR (P857M)
- PROGRAMMABLE REAL TIME CLOCK
- DIRECT, INDIRECT, INDEXED, INDEXED INDIRECT ADDRESSING
- 63 INTERRUPT LEVELS
- EXTERNAL REGISTER TRANSFERS
- HARDWARE MULTIPLY/DIVIDE, DOUBLE LENGTH ARITHMETIC
- AUTOMATIC STACK HANDLING
- REAL TIME CLOCK (20 MS, MAINS)
- INTEGRATED V24 SERIAL CONTROL UNIT
- POWER FAILURE DETECTION WITH AUTOMATIC RESTART
- MICRODIAGNOSTICS
- LOW AND HIGH SPEED DATA CHANNELS
- INTERFACES FOR INDUSTRIAL EQUIPMENT
- DATA COMMUNICATION
- POSSIBILITIES TO CONNECT ALL STANDARD PERIPHERALS
- SOFTWARE PACKAGE INCLUDES:
  STAND ALONE SOFTWARE
  BASIC AND BASIC REAL TIME MONITORS
  DISC AND DISC REAL TIME MONITORS
  MULTI APPLICATION MONITOR (P857M)
  SMALL REAL TIME MONITOR
  CASSETTE OPERATING MONITOR
  MONITOR EXTENSION FOR DATA COMMUNICATION
  ASSEMBLER, FORTRAN COMPILER, BASIC, FACT, LINKAGE EDITOR, OVERLAY LINKAGE EDITOR, CASSETTE EDITOR, UPDATE PACKAGE, LINE EDITOR, DEBUGGING PACKAGE, HARDWARE TEST PROGRAMS

P856M/P857M
System Handbook

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Preface

This handbook is one of a series of manuals which covers all aspects of the P856M and P857M mini computer system. It is intended to provide general information with respect to the system in the form of short descriptions of the component units and peripheral devices which comprise the system.

Because of the flexibility of the system it is possible to include non-standard and customer designed equipment within any system and where such possibilities exist the connection facilities available have also been generally described. A user should however refer to the more detailed publications within the series before using such facilities.

Great care has been taken to ensure that the information contained in this manual is accurate and complete. Should a user, however, find any errors or omissions, or wish to suggest improvements, he is invited to write his comments on the sheet provided at the end of this book and send it to:
Manual Writing Small Computers
at the address on the opposite page.

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Cabinet	– The basic structure containing 19'' racks
Rack	– The structure within the cabinet to which rack mounted units may be secured.
Basic Cabinet	– A cabinet in which the CPU is mounted.
Extension Cabinet	– A cabinet containing system equipment other than the CPU.
Mounting Box	– The rack in which the CPU is plugged.
Equipment Shelf	– The rack in which system equipment other than the CPU is plugged.
Standard Device Unit or Package	– One which is listed in the Catalogue.
Microdiagnostics	– A microprogram standard available on the CPU board, which tests panel drivers, data path, bus dialogue and memory.
Character	– One half-word: 8 bits.
MSI	– Medium Scale Integration.
LSI	– Large Scale Integration.
TTL	– Transistor to Transistor Logic.
ROM	– Read Only Memory.
PROM	– Programmable Read Only Memory.
MOS	– Metal Oxide Semi-conductor.
IPL	– Initial Program Loader.
GP BUS	– General Purpose Bus.
MMU	– Memory Management Unit.
FPP	– Floating Point Processor

The P856M and the P857M mini computers are general purpose digital processors designed for industrial and scientific applications.
These computers are the newest members of the successful P800M series family which were placed in all Western-European countries as well as in the United States and Japan.

The P856M and the P857M are fast, compact and easy to interface thanks to the asynchronous General Purpose Bus around which all I/O facilities are centered and two types of memory available. The P856M is the smaller computer of the two with a maximum of 32k memory. Memory modules for this computer are 8k 16-bit words with a cycle time of 1.2 μs. Also available are 16k 16-bit word memory modules with either 0.7 μs or 1.2 μs cycle time. If two 16k fast memory modules are used memory cycles interleaving is possible.

The P857M offers a tremendous increase in memory size and programming power thanks to a one-board Floating Point Processor and a one-board Memory Management Unit.
The Floating Point Processor gives a hardware execution of floating point instructions. The Memory Management Unit provides the user with two important features: it permits word and character addressing in up to 128k words memory *and* it implements memory protection on a 2k word page basis.
Together with a backing store, such as disc, the system offers a practically unlimited programming space and gives the user all the advantages of a real-time environment, under control of a Multi Application Monitor.
Standard memory modules are 16k 16-bit words with 0.7 μs cycle time. On option, 16k 1.2 μs cycle time memory modules may also be used.
The high speed memory allows interleaving when at least two 16k modules are used.

Standard features for both CPU's are:
- 16 hardware registers of which 14 are fully programmable
- integrated V24 serial control unit
- power failure/automatic restart
- line frequency real time clock (20 ms)
- general purpose bus
- 63 program interrupt levels
- direct access for up to 256 external registers
- direct memory access facility
- microprogrammed standard instruction set
- addressing for up to 32k 16-bit words
- hardware bootstrap loader

plus the following features particular to each CPU:

P856M
- microdiagnostics for automatic and step-by-step testing of the first 4k words of memory and CPU-CU dialogue.
- programmable Real Time Clock (option).

P857M
- microdiagnostics for automatic and step-by-step testing of the first 16k words of memory and CPU-CU dialogue.
- addressing extension for up to 128k words of memory through a Memory Management Unit MMU (option)
- memory protection on a 2k words page basis
- Floating Point Processor (option)
- programmable Real Time Clock (option).

All input/output transfers are handled via the General Purpose Bus. A comprehensive and powerful instruction set, including instructions such as multiply, divide, multiple store, multiple load, external register handling instruction and, for the P857M some extra instructions pertaining to the MMU facility, for table handling and extended memory addressing and the Floating Point Processor provide the programmer with a wide range of programming possibilities and fast execution of programs.

System software for the P856M comprises six monitors:
Basic Operating Monitor, Disc Operating Monitor, Cassette Operating Monitor, Basic Real Time Monitor, Disc Real Time Monitor, Small Real Time Monitor and a monitor extension to be used in a data communication application. The system software for the P857M is the same as for the P856M plus a Multi Application Monitor to be used in systems over 32k words.

Moreover the following processing and service software is available:

Assemblers, Linkage Editors, Overlay Linkage Editor (P857M only), FORTRAN, Real Time FORTRAN, Line Editor, Update Packages, Cassette Update, Debugging Package plus several utility packages.
BASIC (Beginners All purpose Symbolic Instruction Code) and FACT (Facility for Automation, Control and Test) conclude this wide range of software available to the user.

All system software for the P856M and P857M is compatible with the P852M system software except for the extended memory addressing software, which can only be usefully used on the P857M over 32k words.

A diagramatic representation of the system's components and input/output structure are shown by figures 1.1 and 1.2 respectively.

THE SYSTEM

The facilities offered to a user by the P856M and P857M minicomputer systems enable each user to produce a tailor made system to suit his own requirements, and thus avoid the need to purchase facilities which will never be used.

The ease with which a system may be constructed and enhanced, and the overall flexibility of the system are centered around the general purpose bus. This asynchronous bus is used for the interconnection of the system's main components: memory, peripheral device control units, transfer facilities, interrupt facilities and the central processing unit itself. Physically the bus may be of various lengths, to suit any particular configuration, and it consists of those lines required to make correct interconnection and operation between units possible.

Efficient operation of the system is organized by a full range of controlling software in conjunction with the interrupt system. The interrupt system is capable of handling up to 63 hardware levels and operates using the necessary bus lines concurrently and independently of data transfers or bus control operations.

Peripheral connection is also made easier by use of the bus and the availability of up to 64 input/output processor sub-channels for high speed data transfers provides the system with a powerful input/output capability. Organization of the channels is on a priority basis and any number of the channels may be in operation at the same time. Once in operation the input/output processors are able to control a transfer between a device control unit and memory using both the bus and a single break line connected directly between the control unit and the input/output processor controlling the exchange.

The central processing unit, connected within the system via the bus, is normally allocated bus time in accordance with the system requirements. However, the possibility exists for the central processing unit to be given the bus whenever this is necessary for system operation. Processor instructions are available to carry out all the normal arithmetic and logical processes necessary for the operation of the system, both at word and in certain cases character level. Input/output instructions exist for the control and operation of all standard peripheral device control units and, in addition, instructions exist to read and write to external

registers via the General Purpose Bus and, for P857M extended memory addressing, instructions to Move Tables and to load registers with addresses for Page handling. The Floating Point Processor permits the use of hardware for the execution of floating point instructions.

Memories
The memories consist of 1.2 μs or 0.7 μs cycle core memory modules connected via the General Purpose Bus. The 0.7 μs memories allow interleaving. It is possible to mix the 1.2 μs and 0.7 μs memories.

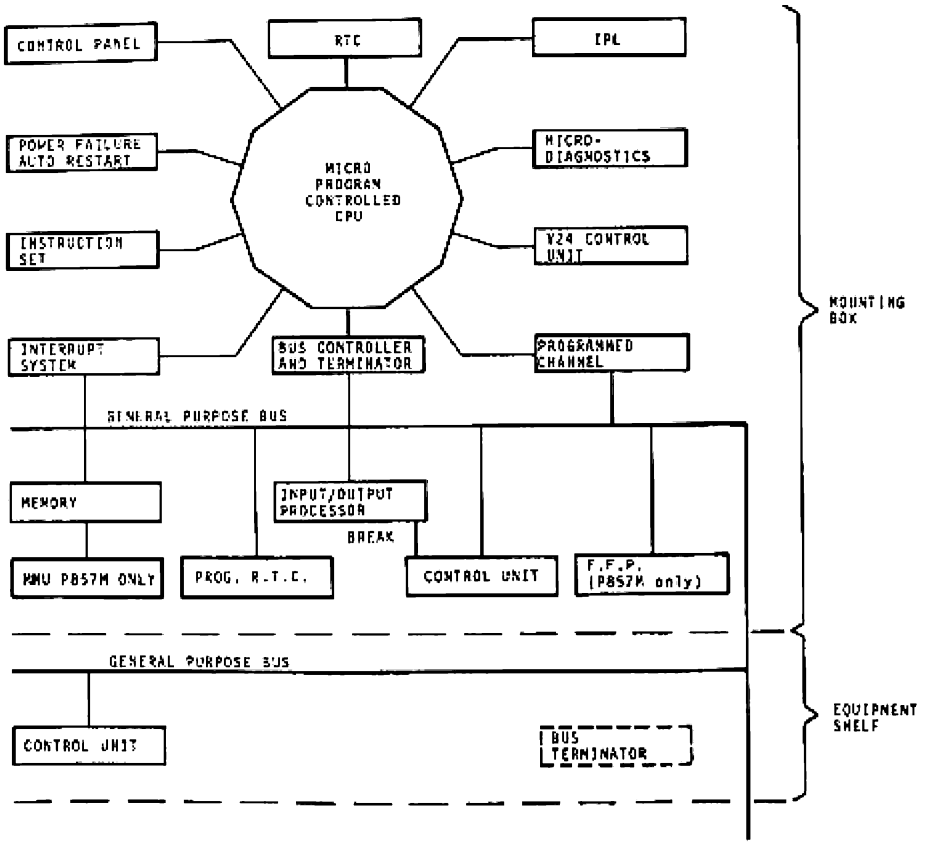


Figure 1.1 System Main Components

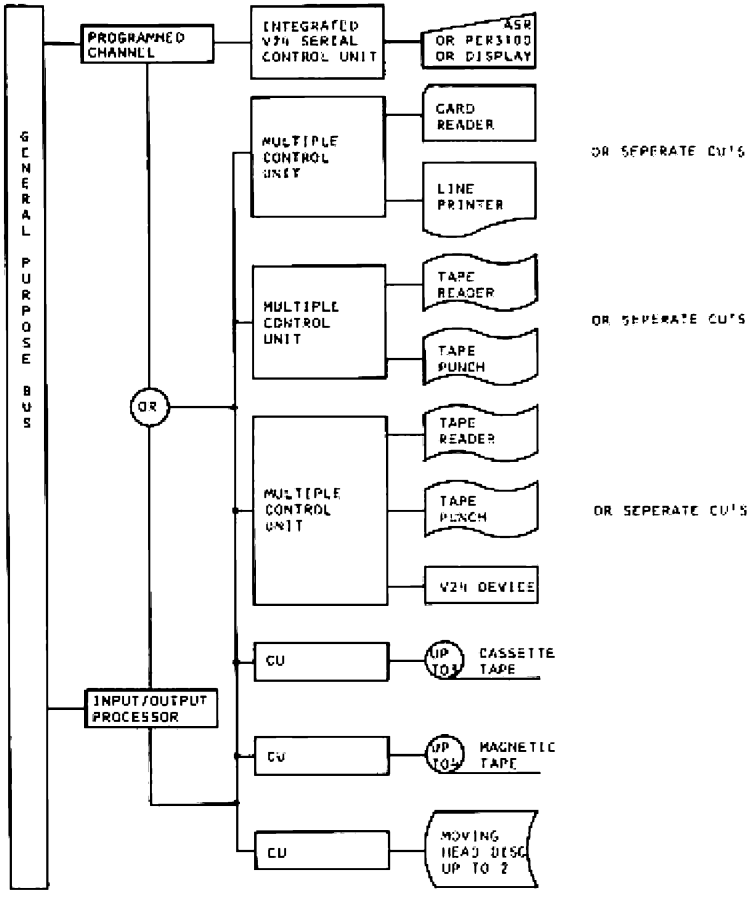


Figure 1.2 Survey of peripherals and their control units

Interleaving

Interleaving of the 0.7 μs read/write core memory permits a very fast execution of instructions. The access time comprises one read cycle after which the execution of the instruction starts immediately. To make full use of the interleaving capability the minimum memory size is 32k i.e. 2 modules of 16k where one module will contain the even addresses and the other module the odd addresses.

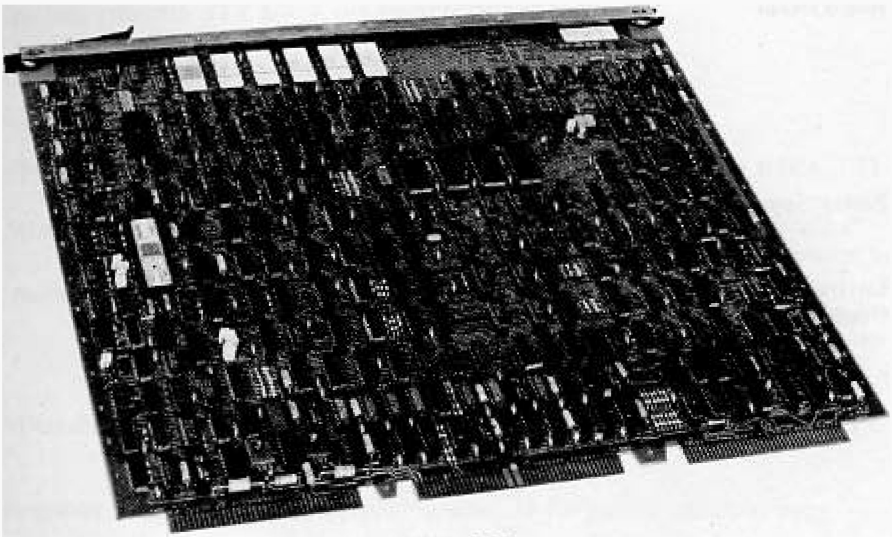
Control Panel
Operator press buttons are provided for normal manual operations, including load and read facilities to both memory and registers and an additional option is available at the control panel to enable the automatic loading and running of a bootstrap program to load any initial program. This bootstrap is held within a ROM fitted on the CPU board and is transferred to memory and executed when the IPL button is pressed.

The main facilities outlined, together with all the normal system and user facilities are covered in more detail in the following chapters.

GENERAL SPECIFICATIONS

CPU Technology	Microprogram controlled processor using ROM, TTL circuitry.
Memory	Coincident current ferrite core memory as standard. The connection of ROM and/or PROM memory is possible. Core memory is available in modules of 8 and 16k for 1.2 μs memories and in modules of 16k for 0.7 μs memories.
Microdiagnostics	Microprogram controlled test for data path, CU-CPU dialogue, memory.
Registers	16 internal registers, 14 for general purpose use.
External Addressing	Addressing possible for up to 64 control units and 256 external registers.
I/O Capability	Up to 64 control units may be connected within the system. Two separate types of transfer channel: 1. Programmed Channel capable of transfer rates up to 30k words/sec. depending on the method of programming used. 2. Up to 8 Input/Output Processor Channels, each controlling up to 8 separate devices on a priority basis and capable of transfer rates up 833k words/sec for memories of 1.2 μs and 1.2Mw with the fast memory. Each device control unit uses a separate break line connected directly between itself and the appropriate input/output processor.

Word Format	16-bit instruction and data word. Data may be handled as two separate 8-bit characters.
Instruction Set	Instructions using 8 different methods of forming an operand, including: - short and long constants - direct and indirect addressing - address and operand in register - indexing
Bus System	Single asynchronous bus using TTL circuitry and incorporating the following subsections: - Bus Control - Data/Command Exchanges - Interrupt Handling - Miscellaneous
Power Supply	100V, 115V, 220V or 240V, 50Hz or 60Hz Standard: 220V 50Hz
Environmental Conditions	0°-45°C, up to 90% relative humidity (without condensation)



P856M CPU

Figure 2.1 shows the main units of the system's hardware structure in block form. Explanations of the memory, GP Bus, interrupt system and input/output facilities are covered in detail in later chapters.

CENTRAL PROCESSING UNIT

The main components of the CPU are:

Arithmetic Unit (ALU)
The circuits which make up this unit enable the addition, subtraction or logical combination of the two 16-bit inputs to be available as a single 16-bit output. In addition the state of the output with reference to a positive, negative, null, or overflow condition is available, and an indication is also given when the ALU output is less than decimal 128 if this output is to be used as a memory address for stack operations. Overall control of the unit is exercised by the micro program held within the system's control ROM.

P Register
This register is used to hold the address of the next instruction to be carried out. It is incremented in steps of two if the program is to carry on in sequence or altered to hold the required new address if a branch is to be carried out. This register is physically only 15 bits, corresponding to bits 0 to 14 of a full 16-bit address word.

The PSW Register
This register is divided into three parts which together form one 16-bit word known as the Program Status Word. Certain instructions and hardware functions cause this word to be stored in a memory stack whenever it is required to be saved. Program action is required to restore the saved word and whilst it is held in the memory stack program action may be carried out to alter the contents of the word.

The PL Register
Six bits used to hold the priority level of the program that is running. Control of this register is exercised by the interrupt system.

The CR Register
Two bits used to hold the state of the result of, or the response to, certain instructions. Control of this register is exercised by the microprogram held within the system's control ROM.

The GF Register
Up to eight bits which are used to record the general status of the system.

The Scratchpad
The scratchpad consists of four 15 × 4-bit read/write memory circuits arranged to give fifteen 16-bit registers A1 to A14, A15. These registers may be addressed from either the instruction being carried out or from switches on the operator's control panel. Overall control of the scratchpad is exercised by the microprogram held within the system control ROM. The specific designation of registers within the scratchpad is:

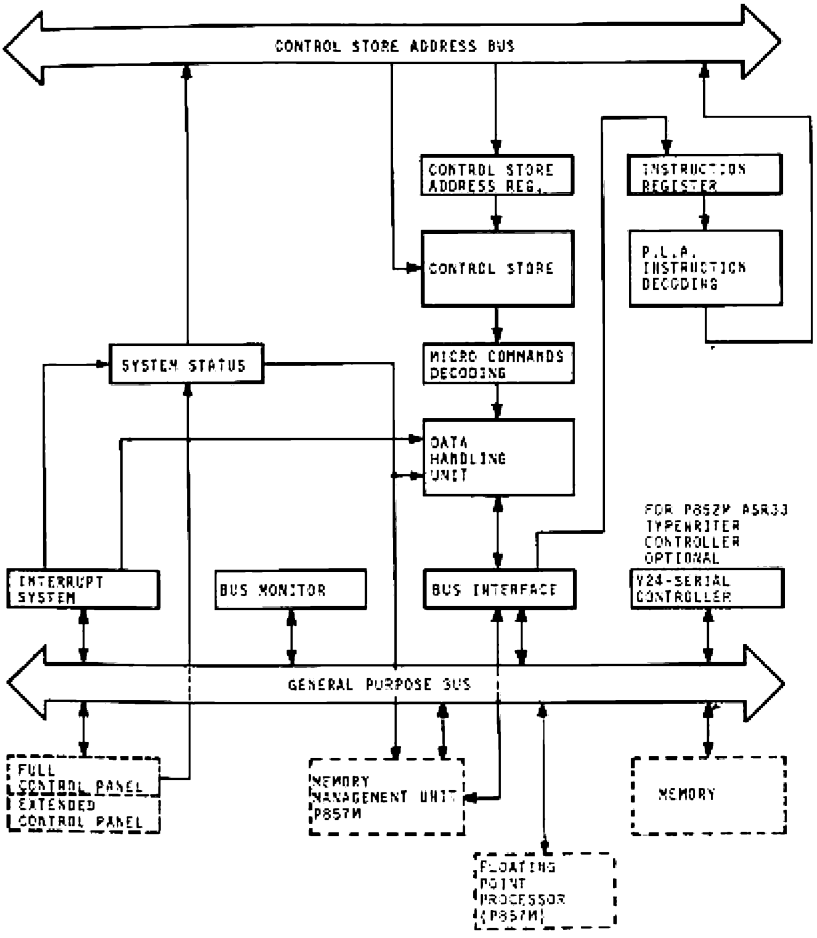


Figure 2.1 General structure of CPU

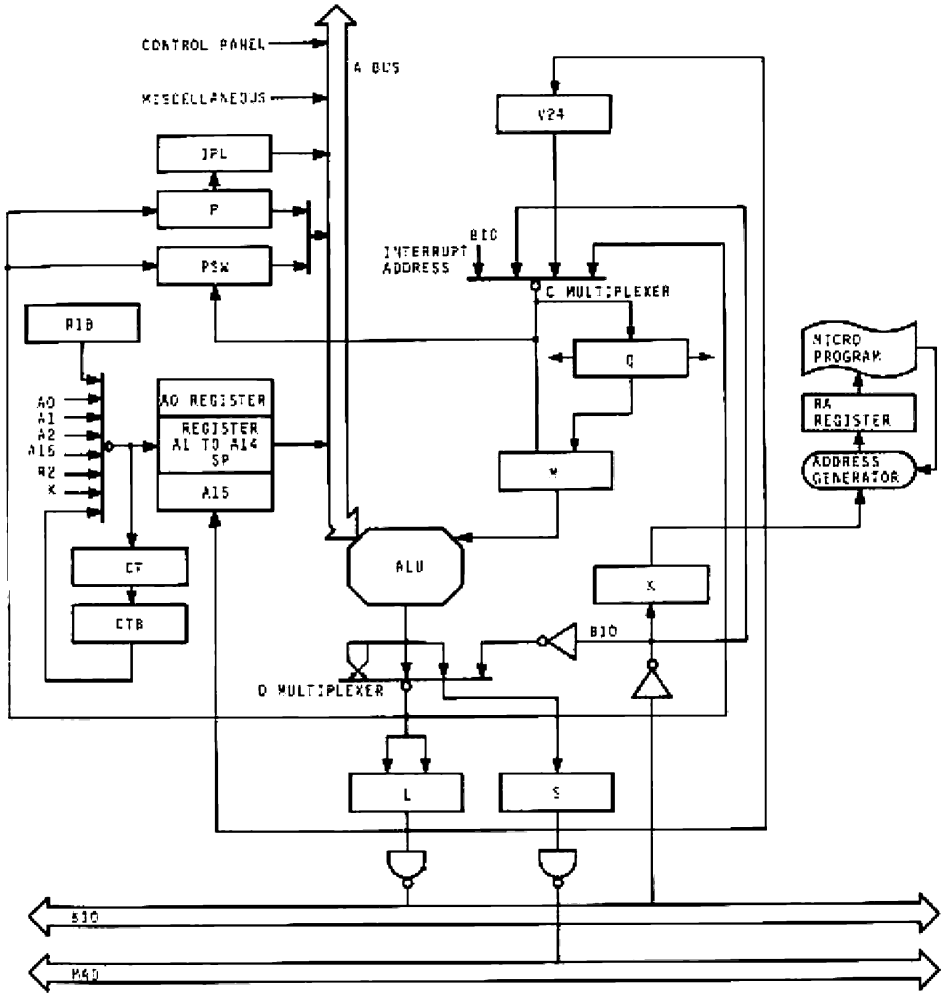


Figure 2.2 Data flow in Data Handling Unit

Registers A1 to A14
These registers are addressed from the instruction format whilst the processor is operating and may be used to hold one or both of the operands of an instruction, and possibly the result. They may also be used as addressing and indexing registers with respect to memory.

Register A15
This register is used as a stack pointer by the interrupt system and as such it is updated whenever it is used for memory addressing. It may also be addressed from the instruction format in the same manner as registers A1 to A14.

The L Register
This 16-bit register is used as a buffer for the output of the ALU. The output from the L register is directed either to the scratchpad or to the general purpose bus, control of the register being exercised by the microprogram held within the system's control ROM.

The M Register
This 16-bit register is used as a multi-purpose register in the input/output-loop of the ALU.

The Q Register
This is a 16-bit register used during double length instruction operations.

The D Multiplexer
This multiplexer has four modes of operation:

ALU output	direct output
	shift right. Input to S Register
	character swap
BUS input	

The C Multiplexer
This multiplexer performs operation on:
- D multiplexer output
- BIO lines output
- Short constant
- Interrupt address
- V24 serializer output

The S Register
This 16-bit register is used as a multi-purpose register by the addressing and counting circuits within the CPU. Control of the register is exercised by the microprogram held within the system's control ROM. The three uses of the S register are:

Normal Addressing
Input to the S register is from the fifteen most significant bits of the output of the ALU. The output of the S register is used for memory, external register, or device addressing, via the general purpose bus. The S register must be reloaded for each change of address.
For the P857M CPU, when running in user mode, only the 12 least significant bits of the S register are sent to the General Purpose Bus, whilst the 4 most

significant bits are sent to the MMU for logical to physical address translation (see page 5-1).
In system mode the 16 bits of the S register are used in the normal way.

Stack Addressing
The S register is initially loaded with the most significant fifteen bits from register A15, via the ALU. It is then used as a downward counter to address consecutive words in the memory stack. Addressing is carried out via the general purpose bus.

Loop Counter
The least significant four bits of the S register are used as a loop counter for use by the system microprogram.

The K Register
This 16-bit register is used to hold either the complete instruction or the most significant word of a double length instruction. It is the contents of this register, together with the current state of the processor, that are used to access the required microprogram words to carry out any instruction and in certain cases bits from the K register are also used directly in the control of instructions. The K register is loaded with the required instruction word from memory via the general purpose bus.

Address Generator GA
The input to the address generator is derived from the K register and the current state of the processor. The unit then encodes the relevant information into the address required by the control microprogram to carry out the particular instruction. The 9-bit output from the generator is input to the RA register.

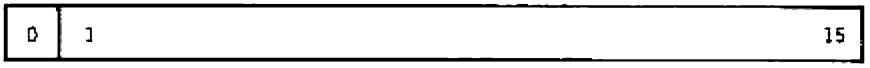
ROM Address Register RA
This 9-bit register buffers the address being used to access the current micro instruction word from the control microprogram. The register is loaded from the output of the address generator and is used directly to address the control ROM.

Control ROM and Microprogram
This section is composed of six ROM ICs. Each IC contains 512 eight-bit words which are accessed by nine addressing inputs. Addressing from the RA register is applied in parallel to the six ICs to obtain 512, fourty-eight bit words of memory.
The microprogram is held in the ROM and exercises direct control over the data paths and timing of the CPU.

Control and Data Flow
The control and data flow of basic instructions is shown in Chapter 8.

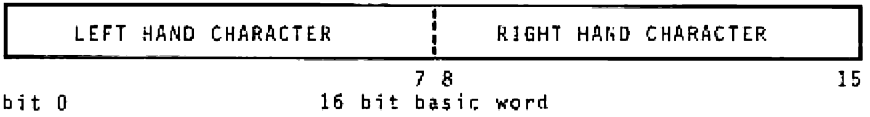
Single Precision

The basic word used within the system is 16 bits, and as such it may be represented by four hexadecimal symbols in the range 0000 to FFFF. Bits within the word are numbered from 0 to 15, bit 0 being the most significant bit. Data may be represented as single precision signed integer contained in one word as follows:



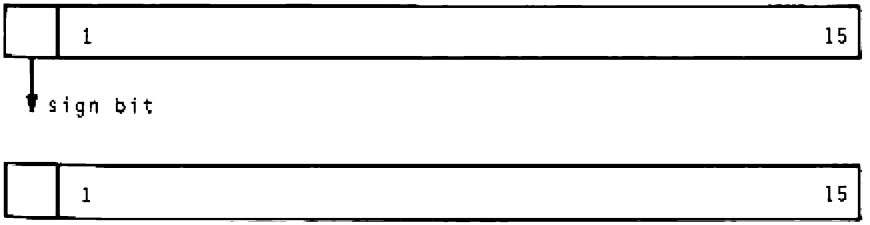
where bit 0 is used as the sign bit, set to zero for positive data and to 1 for negative data.

For programming purposes the word may be divided into two 8-bit characters which may be used independantly by certain processor actions, bits 0 to 7 of the word representing the left hand character and bits 8 to 15 representing the right hand character.



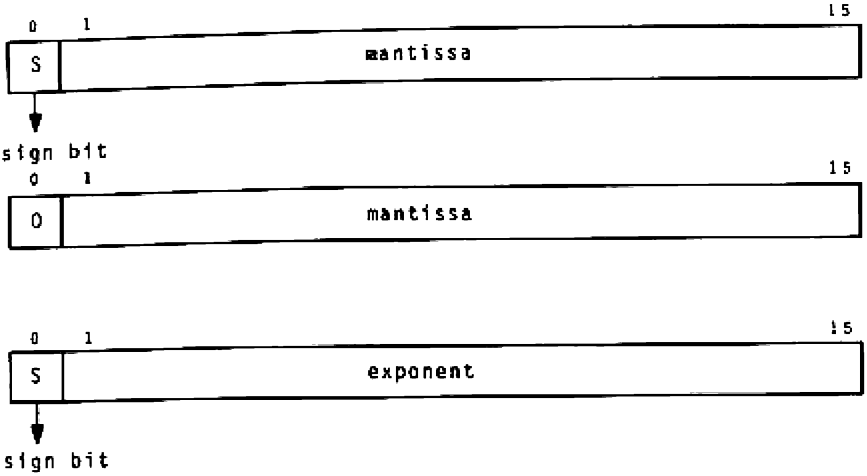
Double Precision

In double length instructions data may also be represented as a double precision signed integer, contained in two words as follows:



The sign bit of the least significant word is not used and is usually set to 0. This means that 30 bits are available for data representation.

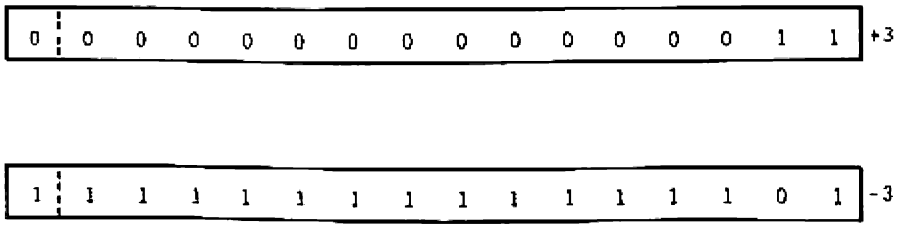
Floating Point Data
Real numbers are place in three successive words. The first two contain the mantissa and the third the exponent.



For a more detailed description see also chapter 6 on the Floating Point Processor.

DATA FORMAT

Data within a word may take the form of numeric values, logical data, or character representation. Within a word positive and negative numeric values are able to be represented, the most significant bit, bit 0, of the word being used to indicate the sign of any value. Positive values are represented by making the sign bit equal to 0 and using the remaining fifteen bits to express the numeric value in binary. Negative values are represented by making the sign bit equal to 1 and expressing the required numeric value by its 2's complement in the remaining fifteen bits.
The figure below shows the representation of the numeric values +3 and −3 within the data word.



Representation of Numeric Values

Numeric values represented and used within characters may only specify positive values to a maximum of 8 binary bits, no sign bit being used by either character.

Logical data may be held and used in either whole word or character format and no sign bit is used, data being bit significant within the complete word or character.

Data representing standard alphanumeric and control characters may be held within the separate characters of the data word and will be treated as either numeric values or logical data depending on the instructions carried out when using such data.

Core memory is available in modules of 8k or 16k 16-bit words with a cycle time of 1.2 μs or 0.7 μs up to maximum of 32k for the P856M and 128k for the P857M. Each module consists of a single printed circuit board which is mounted within the mounting box. Connection to the system is by pluggable connectors to the General Purpose Bus and provision is made for the protection from loss or detorioration of data during power on/off sequences and in the event of any power failure.

All memory modules offered are able to operate in either word or character mode and special character handling instructions are available to provide a useful and efficient facility with respect to character buffering and transfers. Character mode operation enables the contents of the least significant eight input/output lines to be either set from, or written into either the left hand or right hand character of the addressed memory location. In all such operations the unused character is left unaltered.

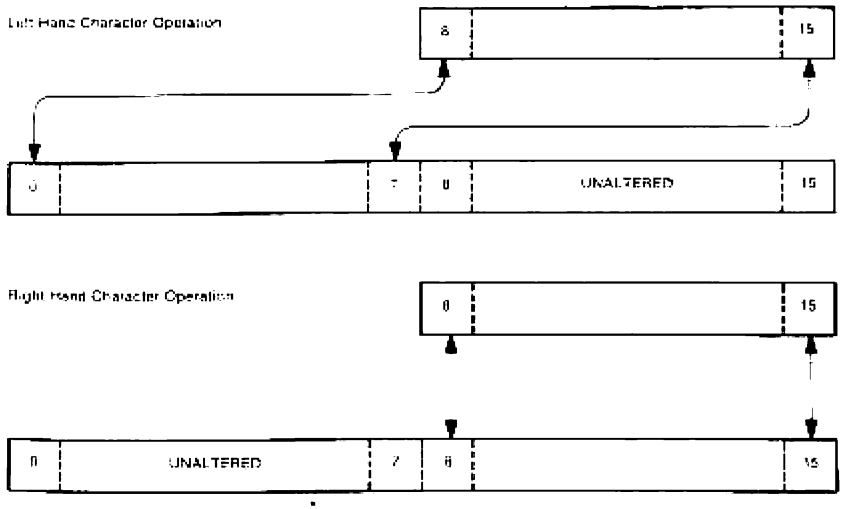
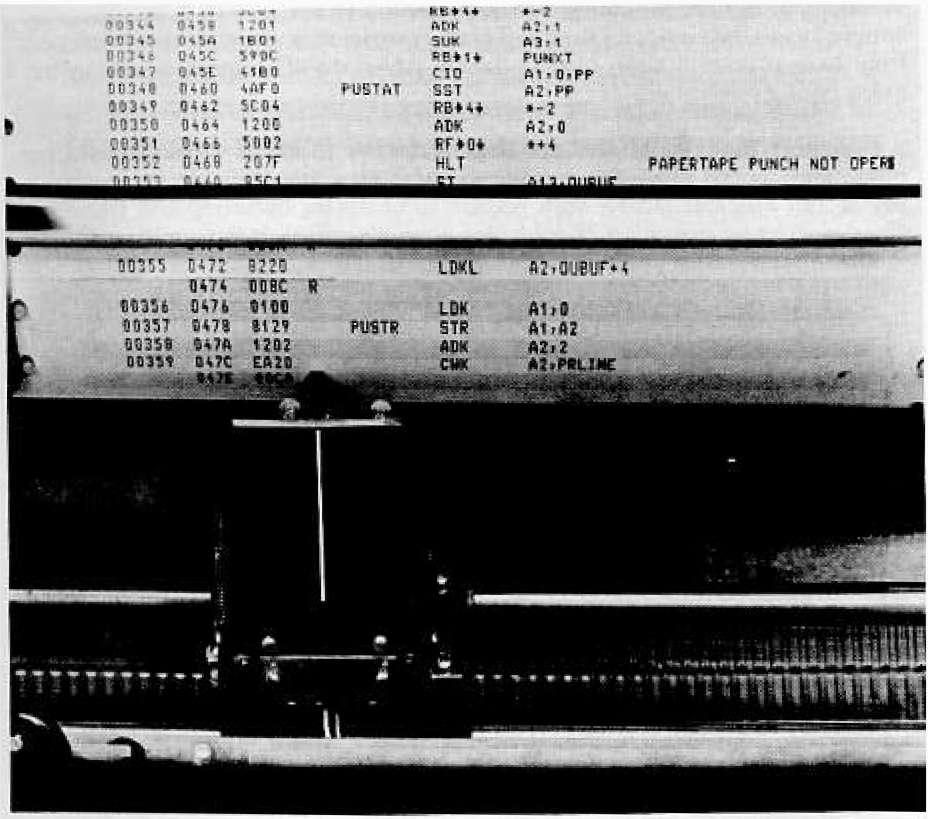


Figure 4.1 Operation of memory in character mode



Listing on PER 3100 matrix printer.

MEMORY ADDRESSING

Depending upon the type of instruction or operation being carried out the memory may be addressed in words or characters for programming purposes. Bits 0 to 14 of the address are used to access memory in word mode, bit 15 being unused and insignificant. When operating in character mode all sixteen address bits are used, bits 0 to 14 addressing the word location required and bit 15 addressing the character. With bit 15 set to 0 the left hand character is addressed, bit 15 set to 1 addresses the right hand character.

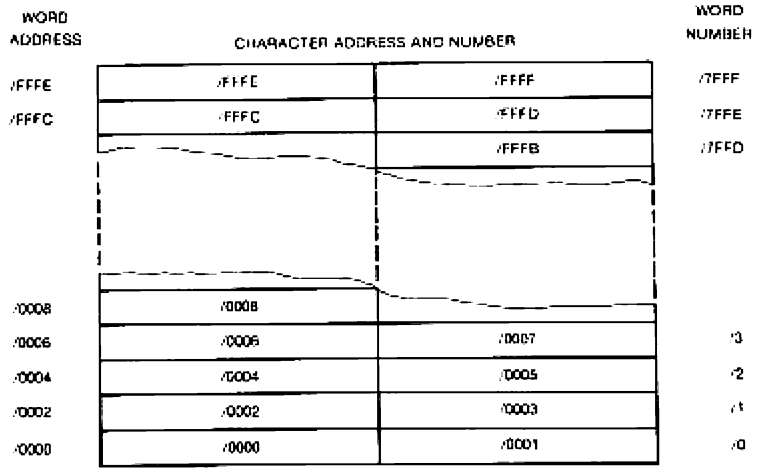


Figure 4.2 Layout of words and characters in memory.

Word addresses written with the least significant bit present will be addressed ignoring this bit.

Memory addressing in an environment >32k is entirely transparent to the user and is taken care of by the Memory Management Unit.

DESCRIPTION

The Memory Management Unit is a feature of the P857M computer which uses Virtual Addressing and allows to extend memory addressing over 32k op to 128k words. It permits dynamic program relocation in multitask programming under control of the Multi Application Monitor and offers a memory protection facility.
The MMU cannot by used with the P856M.
Special instructions are required by the MMU to handle the memory addressing.

The system considers the memory as consisting of n blocks of 2k words, called pages. The monitor is always loaded at the beginning of memory from the lowest address upwards. When the user program is called it is loaded behind the monitor and it is split in pages of 2k, which do not need to be contiguous. Moreover, only those parts of the program are loaded which are required at the time.
A user program may not exceed 32k words.

In order to address the pages in memory a segment table of 16 × 16 bits is built for each program called.
The user program uses relative addresses contained in 16 bits. At execution time these logical addresses are divided in two parts. One part, bits 0 to 3 included, contain a segment address and bits 4 to 15 included contain the relative address from the beginning of the page.
The segment address refers to an entry in the segment table and the MMU translates the entry, pointed to by the 4-bit segment address, into a 6-bit physical page number which, together with the 12-bit displacement value, produces an 18-bit address.

If the running program has less than 16 pages loaded in memory the unused words of the segment table have a protection bit set.

In system mode, see page 13-10, the MMU does not translate the 4-bit segment addresses as the system software routines use absolute addresses.
To transfer in this mode data from a system to a user area special instructions which have a source table address, destination address and length as parameters, permit to communicate between the user and system areas.

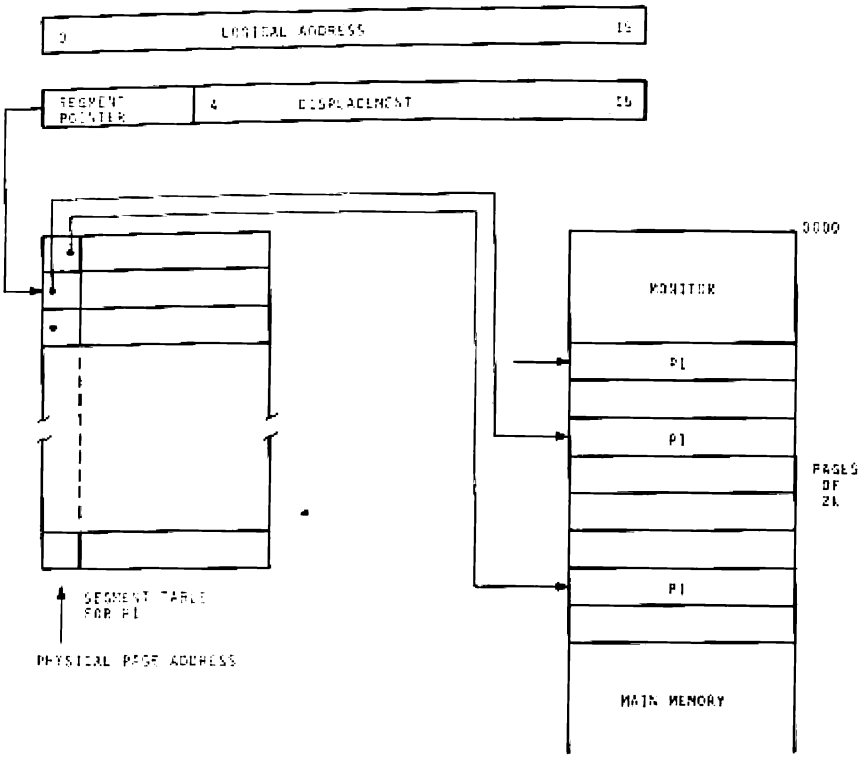


Figure 5.1 MMU Operation.

Layout of segment table word

The MMU and the operating system control the contents of the segment table words. The bits in this word have the following meaning:

bits 0-5	Physical Page address.
bit 6	Page Error indication. This bit is set by the Operating System for those pages which do not belong to the addressing environment of the running program. By checking this bit the MMU activates a 'Page Fault' signal when a wrong or missing page is tried to be accessed. This bit is not used for system programs.
bit 7	Read Only page. This bit is set when the relevant page is protected against overwriting. This feature allows to share the page among several user programs.

bit 8 Modified Page. This bit is set by the MMU when a write operation took place in this page. If so, the page need to be swapped out again to the backing store before a new page is loaded. If the bit remains zero the page may be overwritten which saves time.

bit 9 Overflow. The setting of this bit depends on the value in bits 10-15 included.

bits 10-15 Counter. A 6-bit counter is associated with each page descriptor. All counters are incremented at regular time intervals. This interval, which depends on the memory speed, is chosen at system generation time in a ratio 1 to 256. During execution of a program, each time a page of the running program is called the counter is reset to zero. If a counter reaches the interval set an overflow bit is set. When space in memory is required the Operating System swaps out those pages which have the overflow bit set.

Page Fault handling

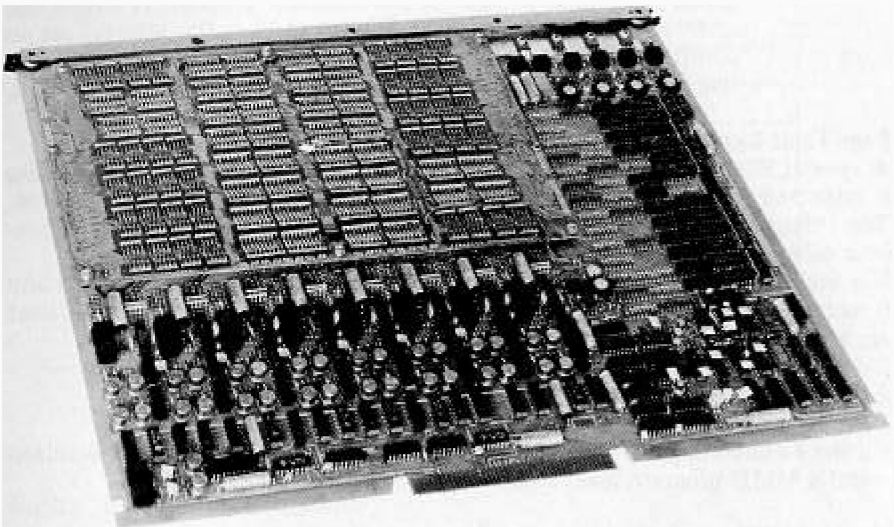
A special interrupt *Page Fault* is given when an attempt is made to write into a protected page or when a missing or wrong page is tried to be accessed. The interrupt line is wired from the MMU to the CPU and it has a priority over other internal or external interrupts.

If a fault is detected the execution of the running instruction is stopped and if necessary, exchange parameters are updated to resume the execution later on. Moreover three words are stored in the system stack:

- the address of the instruction which caused the page fault interrupt
- the PSW
- a word containing the page address of the page in which a fault was detected and a MMU program level coded on the MMU board.

Next the CPU is switched to the Inhibit state and the computer to system mode. The MMU program level is loaded in the PLR register and a branch is made to an interrupt routine address.

The interrupt routine does not require an RIT instruction to reset the interrupt as the Page Fault interrupt is automatically deactivated.



16k Memory Module 1.2 μs

Introduction

The Floating Point Processor is an optional, high speed arithmetic processor which may be included in the P857M system.
It performs by hardware, single precision, all floating point arithmetic operations.
The processor is contained on one board and must be plugged in the *third* slot of the M4 or M5 mounting box, also when no Memory Management Unit is used. The power consumption is + 5 V, 6.0 Amps.
Figure 6.1 shows the connection of the FPP in the system.

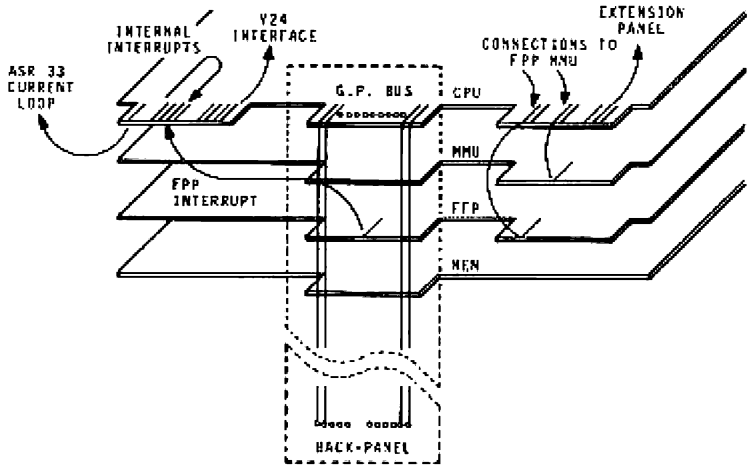


Figure 6.1 Connection of Floating Point Processor

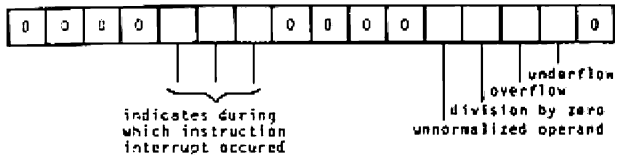
Operation

The board contains three 16-bit accumulators FPA holding the result of a floating point operation or the floating point operand or the first floating point operand where the second floating point operand is temporarily placed in three other 16-bit registers.

Program instructions are fetched and decoded by the CPU. The significant bits of each instruction, i.e. op.code, mode, bits etc. are also copied in an instruction register on the FPP board.
When a floating point instruction is encountered in the program the Floating Point Processor is activated by the CPU and the latter stops.
Some decoding of the instruction register contents takes place on the FPP board

and an arithmetic unit on this board is signalled the type of operation it has to perform.
The arithmetic unit takes the information to be operated upon from the contents of the FPA, registers A1 and A2, the contents of consecutive memory locations.

The result is stored in FPA, or A1 and A2, or a number of consecutive memory locations.
During or immediately after the execution a status register is reset to either zero (no errors) or bits in this register are set to 1. The contents of the status register may be:



Any abnormal condition gives an FPP interrupt and sets the CPU condition register to 3. The FPP interrupt must be connected to one of the eight internal interrupt levels.
If no error condition was obtained the CPU fetches the next instruction.
Figure 6.2 gives the architecture and flow in the FPP.

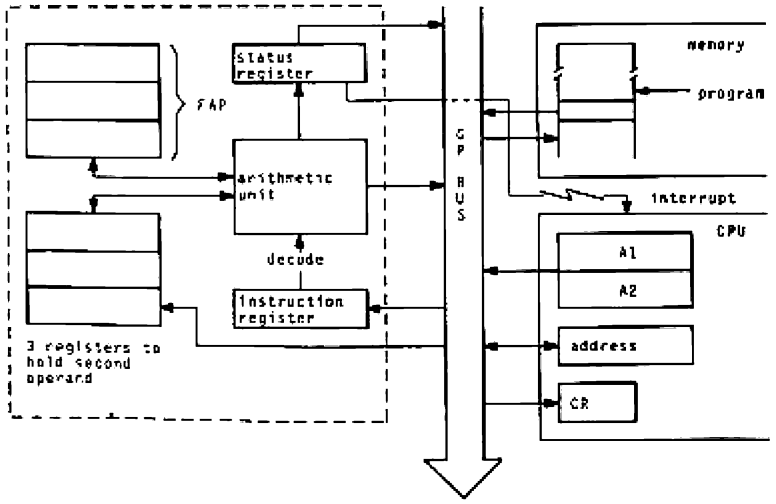
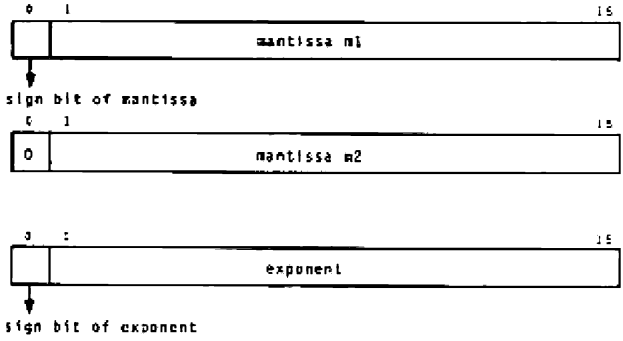


Figure 6.2 Floating Point Processor

Floating Point Format
The Floating Point Processor handles data of the following format:

Floating Point Data
Floating Point Data are real numbers contained in three consecutive 16-bit words. The first two words contain the mantissa which is a left normalized, double precision number.
The exponent is held in the third word as a single precision integer.



The sign bit of the second mantissa word is always zero.
The mantissa scale is between:

positive: $+ \frac{1}{2} \leq m < 1 - \varepsilon$

where $\varepsilon = 2^{-30}$

negative: $-1 \leq m < -\frac{1}{2} - \varepsilon$

The exponent scale is between: $-2^{15} \leq E < +2^{15} - 1$

A floating point number is: $(m1,m2) \times 2^E$, where E = the exponent.
The absolute value is: | DATA | $< 10^{9868}$. The accuracy is in 9 decimal digits.

The Floating Point Processor also allows the conversion of floating point data to integer format and vice versa.
In that case the Processor permits operations with single precision integers (on 16 bits) and double precision integers (on 32 bits, the most significant bit of the second word being 0).

Floating Point Instructions

Floating Point Instructions use the same type of addressing modes as the remainder of the P857M instruction set.

A survey of the Floating Point Instruction Set is:

FFL Convert the double precision integer to a floating point operand. Store the result in FPA.

FFX Convert a floating operand in FPA to a double precision integer. The result is placed in A1 and A2.

FADR Add the floating point operand in FPA to the floating point operand in three consecutive memory locations. The first address is indicated by the contents of the specified register. The result is either placed in FPA or in memory.

FAD Add the floating point operand in FPA to the floating point operand in three consecutive locations. The first address is indicated by the address in the instruction. The result is placed in FPA or in memory.

FSUR Subtract the floating point operand in three consecutive memory locatons, the first address is indicated by the register in the instruction, from the floating point operand in FPA. The result is placed in FPA or in memory.

FSU Subtract the floating point operand in three consecutive memory locations, the first address is given by the address in the instruction, from the floating point operand in FPA. The result is placed in FPA or in memory.

FMUR Multiply the floating point operand in FPA by the floating point operand in three consecutive memory locations, whose first address is given by the register in the instruction. The result is stored in FPA or in memory.

FMU Multiply the floating point operand in FPA by the floating operand in three consecutive memory locations, whose first address is pointed to by the address in the instruction. The result is stored in FPA or in memory.

FDVR Divide the floating point operand in FPA by the floating point operand in three consecutive memory locations, whose first address is given in the register specified in the instruction. The result is placed in FPA or in memory.

FDV Divide the floating point operand in FPA by the floating point operand in three consecutive memory locations, whose first address is pointed to by the address in the instruction. The result is placed in memory or in FPA.

FLDR The contents of three consecutive memory locations are placed in FPA. The first memory location is indicated by the register in the instruction.

FLD The contents of three consecutive memory locations are placed in FPA. The first memory location is pointed to by the address in the instruction.

FSTR The contents of FPA are stored in three consecutive memory locations. The first address is indicated in the register in the instruction.

FST The contents of FPA are stored in three consecutive memory locations. The first location is pointed to by the address in the instruction.

See Chapter 7 for instruction execution times.

The instruction set gives the programmer the ability to carry out all the functions necessary to program the system efficiently and may be divided into ten basic groups:

Load/Store Instructions
Arithmetic Instructions
Logical Instructions
Character Instructions
Branch Instructions
Shift Instructions
Control Instructions
Input/Output Instructions
External Transfer Instructions
Move Table Instructions

Within these groups efficiency is ensured by the possible use of up to eight different methods of forming one of the instruction's operands, the method to be used being chosen by the programmer with reference to the memory and timing requirements of any particular program.

Two formats for instruction layouts are used and where necessary two words are used to define an instruction.

INSTRUCTION FORMATS

Two instruction formats are possible and these are defined within the instruction by the most significant bit, bit 0, of the instruction word. Where instructions consist of two words the format bit is the most significant bit of the first word only.

Format 0 instructions are always short, that is one word. Format 1 instructions may be short or long, one or two words.

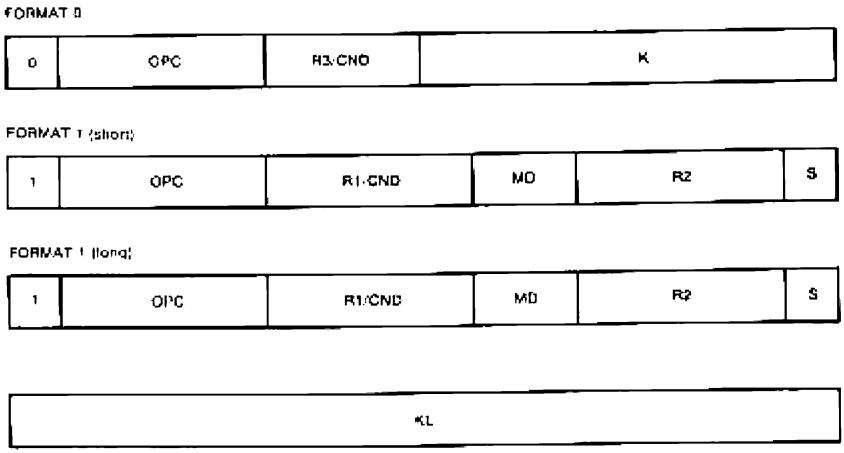


Figure 7.1 Layout of instruction formats.

OPC 4 bits, the pattern of which defines the instruction to be carried out.

R1 4 bits, specifies the working register to be used by the instruction, A0 - A15. It may contain one of the operands to be used and may also be used to hold the result of the instruction. In certain cases with R1 = 0 the addressed register, the P register, will not be used and in these cases R1 = 0 will qualify the operation code and define a different instruction than when R1 = 0.

R2 4 bits, specifies the second working register to be used by the instruction A1 - A15. It may contain the second operand or hold an address to be used in forming this operand. If R2 is made zero, no second working register is specified but this condition is used in deciding the method of forming the second operand.

R3 3 bits, specifies the working register to be used by the instruction A0 - A7. It may contain one of the operands to be used and may also be used to hold the result of the instruction. In certain cases with R3 = 0 the addressed register, the P register, will not be used and in these cases R3 = 0 will qualify the operation code and define a different instruction than when R3 = 0.

CND 3 bits, specifies the condition which must exist for a particular instruction to be carried out. Used to qualify conditional branch instructions and replaces R3 or the most significant 3 bits of R1.

MD 2 bits, specifies the mode of addressing to be used when forming the second operand of an instruction where this is applicable.

S 1 bit, applicable to certain instructions using memory. When present it specifies that the result of the instruction concerned is to be stored in the memory address specified by the instruction. When this bit is not present the result is placed into the working register specified by R1.

K 8 bits, these bits are used to specify the operand in format 0 instructions, and include short constant operands (k) and short displacements (m-for relative branch instructions). This field is also used to specify counts for shift instructions (n) and device addresses to I/O instructions (dev), in these cases a part of the field may be used to qualify the operation code.

KL 16 bits, this field is made up of the complete second word of a double length instruction and may specify a long constant (KL) or an address (m).

FORMING THE OPERAND

Many of the instructions may use various methods of forming one of the operands to be used. In all, eight methods of forming an operand are available governed by the values of the Format, Mode, and R2 fields of the instruction layout.

Figure 7.2 lists the eight methods of forming an operand and a brief description of each method is given following the figure.

Type	Format	Mode	R2	
T1	1	00	–	Reg/Reg.
T2	1	01	R2 = 0	Long Constant
T3	1	01	R2 ≠ 0	Address in Reg R2
T4	1	10	R2 = 0	Address in next word
T5	1	10	R2 ≠ 0	Indexed
T6	1	11	R2 = 0	Indirect
T7	1	–	R2 ≠ 0	Indexed Indirect
T8	0	–	–	Short Constant

Figure 7.2

T1. Register/Register - Format 1 (short)
The operand is the value in the register specified by R2 of the instruction format.

T2. Long Constant - Format 1 (long)
The operand is the value in the least significant word, all sixteen bits, of the double length instruction format.

T3. Address in Register - Format 1 (short)
The operand is held in memory. The memory address of the operand is the value in the register specified by R2 of the instruction format.

T4. Address in Next Word - Format 1 (long)
The operand is held in memory. The memory address of the operand is the value in the least significant word of the double length instruction.

T5. Indexed Address in Next Word - Format 1 (long)
The operand is held in memory. The memory address of the operand is found by adding the value in the register specified by R2 of the instruction format to the value in the least significant word of the double length instruction.

T6. **Indirect Address in Next Word – Format 1 (long)**
The operand is held in memory. The memory address of the operand is also held in memory. This indirect address is the value in the least significant word of the double length instruction.

T7. **Indexed Indirect Address in Next Word – Format 1 (long)**
The operand is held in memory. The memory address of the operand is also held in memory. This indirect address is found by adding the value in the register specified by R2 of the instruction format to the value in the least significant word of the double length instruction.

T8. **Short Constant – Format 0**
The operand is the value in the least significant eight bits of the instruction format.

INSTRUCTION TIMING

The timing of the instructions depends on various factors: the type of instruction itself, the memory, the method of forming the operand and the number of memory cycles required.
The instruction set offers the possibility of very rapid execution times where single word register/register or short constant operations are employed whilst the more complex register/memory instructions save execution time when compared with the routines they may replace.
Execution time is also reduced in the case of conditional instructions by carrying out the conditional check immediately after accessing the instruction and then only continuing if the required conditions are satisfied.

TRAP ACTION

The use of any invalid instruction causes the activation of the Trap action which consists of the following basic actions:
- the CPU does not attempt to carry out the instruction
- information with reference to the instruction address and processor status is saved in the stack
- interrupts are inhibited
- a user mode flag is reset when working in user mode
- an indirect branch is made to address /7E for a trap routine.

THE INSTRUCTION SET

The instructions within the basic groups, together with their mnemonic, addressing type(s) and the execution time for the different types of memory are listed here:

Load/Store Instructions		Addressing types	Execution times in μs	
			1.2 μs memory	0.7 μs memory
LD	Load	T4 - T7	3.7 - 5.0 μs	2.2 - 3.0 μs
LDR	Load Register	T1, T3	1.4 - 2.5 μs	1.2 - 1.8 μs
LDK	Load Constant	T8, T2	1.3 - 2.5 μs	0.9 - 1.5 μs
ST	Store	T4 - T7	3.8 - 5 μs	2.4 - 3.3 μs
STR	Store Register	T3	2.8 μs	2.1 μs
ML	Multiple Load	T4 - T7	2.8 - 4.1 + nx1.3 μs	2.6 - 3.5 + nx0.8 μs
MLR	Multiple Load Register	T3	2.0 - 2.4 + nx1.3 μs	1.9 - 2.3 + nx0.8 μs
MLK	Multiple Load Constant	T2	2.9 + nx1.3 μs	2.7 + nx0.8 μs
MS	Multiple Store	T4 - T7	2.8 - 4.1 + nx1.3 μs	2.6 - 3.5 + nx0.8 μs
MSR	Multiple Store Register	T3	2.5 - 3.1 + nx1.3 μs	2.3 - 2.9 + nx0.8 μs
EL	Extended Load (MMU)	T4 - T7	3 - 4.1 μs	2.4 - 3.3 μs
ELR	Extended Load Register (MMU)	T3	2.5 μs	2.1 μs
ES	Extended Store (MMU)	T4 - T7	3 - 4.1 μs	2.4 - 3.3 μs
ESR	Extended Store Register (MMU)	T3	2.5 μs	2.1 μs
Arithmetic Instructions				
AD	Add	T4 - T7	3.8 - 6.3 μs	2.2 - 3.9 μs
ADR	Add Register	T1, T3	1.4 - 3.8 μs	1.2 - 2.6 μs
ADK	Add Constant	T8, T2	1.3 - 2.5 μs	0.9 - 1.5 μs
SU	Subtract	T4 - T7	3.8 - 6.3 μs	2.2 - 3.9 μs
SUR	Subtract Register	T1, T3	1.4 - 3.8 μs	1.2 - 2.6 μs
SUK	Subtract Constant	T8, T2	1.3 - 2.5 μs	0.9 - 1.5 μs
MU	Multiply	T4 - T7	9.7 - 11 μs	8.6 - 9.5 μs
MUR	Multiply Register	T1, T3	7.8 - 8.5 μs	7.6 - 8.9 μs
MUK	Multiply Constant	T2	8.5 μs	7.9 μs
DV	Divide	T4 - T7	10 - 11.3 μs	8.8 - 9.5 μs
DVR	Divide Register	T1, T3	7.8 - 8.8 μs	7.6 - 8.9 μs
DVK	Divide Constant	T2	8.8 μs	8.2 μs

		Addressing types	Execution times in μs	
			1.2 μs memory	0.7 μs memory
DA	Double Add	T4 - T7	5.6 - 6.9 μs	3.9 - 4.8 μs
DAR	Double Add Register	T1, T3	3.1 - 4.5 μs	3.0 - 3.6 μs
DAK	Double Add Constant	T2	4.4 μs	3.2 μs
DS	Double Subtract	T4 - T7	5.6 - 6.9 μs	3.9 - 4.8 μs
DSR	Double Subtract Register	T1, T3	3.1 - 4.5 μs	3.0 - 3.6 μs
DSK	Double Subtract Constant	T2	4.4 μs	3.2 μs
C2	Two's Complement	T4 - T7	5.3 - 6.5 μs	3.5 - 4.4 μs
C2R	Two's Complement Register	T3	4.0 μs	3.1 μs
IM	Increment Memory	T4 - T7	5.0 - 6.3 μs	3.0 - 4.0 μs
IMR	Increment Memory Register	T3	3.8 μs	2.6 μs
NGR	Negate Register	T1	2.0 μs	1.9 μs
CM	Clear Memory	T4 - T7	3.8 - 5.0 μs	2.4 - 3.3 μs
CMR	Clear Memory Register	T3	2.8 μs	2.1 μs
CW	Compare Word	T4 - T7	3.8 - 5.0 μs	2.2 - 3.0 μs
CWR	Compare Word Register	T1, T3	1.4 - 2.5 μs	1.2 - 1.8 μs
CWK	Compare Word Constant	T2	2.5 μs	1.5 μs
FFL	Integer to Floating Point	T1		3.7 µs
FFX	Floating Point to Integer	T1		5.1 µs
FAD	Floating Point Addition	T4-T7		6.2 - 9.6 µs
FADR	Floating Point Addition/Register	T3		5.9 - 8.4 µs
FSU	Floating Point Subtract	T4-T7		6.2 - 9.6 µs
FSUR	Floating Point Subtract/Register	T3		5.9 - 8.4 µs
FMU	Floating Point Multiply	T4-T7		8.8 - 12.2 µs
FMUR	Floating Point Multiply/Register	T3		8.4 - 11.0 µs

		Addressing types	Execution times in μs	
			1.2 μs memory	0.7 μs memory
FDV	Floating Point Division	T4-T7		8.8 - 12.2 µs
FDVR	Floating Point Division/Register	T3		8.4 - 11.0 µs
Logical Instructions				
AN	Log. AND	T4 - T7	3.8 - 6.3 μs	2.2 - 3.9 μs
ANR	Log. AND Register	T1, T3	1.4 - 3.8 μs	1.2 - 2.6 μs
ANK	Log. AND Constant	T8, T2	1.3 - 2.5 μs	0.9 - 1.5 μs
OR	Log. OR	T4 - T7	3.8 - 6.3 μs	2.2 - 3.9 μs
ORR	Log. OR Register	T1, T3	1.4 - 3.8 μs	1.2 - 2.6 μs
ORK	Log. OR Constant	T8, T2	1.3 - 2.5 μs	0.9 - 1.5 μs
XR	Exclusive OR	T4 - T7	3.8 - 6.3 μs	2.2 - 3.9 μs
XRR	Ex. OR Register	T1, T3	1.4 - 3.8 μs	1.2 - 2.6 μs
XRK	Ex. OR Constant	T8, T2	1.3 - 2.5 μs	0.9 - 1.5 μs
TM	Test Mask	T1	1.4 μs	1.2 μs
TNM	Test Not Mask	T1	1.4 μs	1.2 μs
CI	One's Complement	T4 - T7	3.8 - 6.3 μs	2.2 - 3.9 μs
CIR	One's Complement Register	T1, T3	1.4 - 3.8 μs	1.2 - 2.6 μs
Character Handling Instructions				
LC	Load Character	T4 - T7	3.8 - 5.0 μs	2.7 - 3.6 μs
LCR	Load Character Register	T3	2.8 μs	2.4 μs
LCK	Load Character Constant	T2	2.8 μs	2.4 μs
SC	Store Character	T4 - T7	3.8 - 5.0 μs	2.4 - 3.3 μs
SCR	Store Character Register	T3	2.8 μs	2.1 μs
CC	Compare Character	T4 - T7	3.8 - 5.0 μs	2.7 - 3.6 μs
CCR	Compare Char. Register	T3	2.8 μs	2.3 μs
CCK	Compare Char. Constant	T2	2.8 μs	2.3 μs
ECR	Exchange Char. Register	T1	1.4 μs	1.2 μs
Branch Instructions				
AB	Absolute Branch	T8, T2	1.3 - 2.1 μs	0.9 - 2.0 μs
ABR	Absolute Branch Register	T1, T3	1.6 - 2.6 μs	1.2 - 2.4 μs
ABI	Absolute Branch	T4 - T7	4.0 - 5.2 μs	1.1 - 3.2 μs

		Addressing types	Execution times in μs	
			1.2 μs memory	0.7 μs memory
RB	Relative Backward Branch	T8	1.3 μs	1.1 μs
RF	Relative Forward Branch	T8	1.3 μs	1.1 μs
CF	Call Function	T2	4.8 μs	4.0 μs
CFR	Call Function Register	T1, T3	4.2 - 4.9 μs	3.6 - 4.1 μs
CFI	Call Function	T4 - T7	5.5 - 6.6 μs	4.5 - 5.4 μs
RTN	Return	T3	3 - 4.4 μs	2.7 - 4.1 μs
EX	Execute	T4 - T7		
EXR	Execute Register	T1, T3	depends on instruction in operand	
EXK	Execute Constant	T2		
Shift Instructions				
SLA	Left Arithmetic Shift	T8	2.0 + nx0.3 μs	1.9 + nx0.3 μs
SRA	Right Arithmetic Shift	T8	1.9 + nx0.3 μs	1.7 + nx0.3 μs
SLL	Left Logical Shift	T8	1.9 + nx0.3 μs	1.7 + nx0.3 μs
SRL	Right Logical Shift	T8	1.8 + nx0.3 μs	1.6 + nx0.3 μs
SLC	Left Circular Shift	T8	1.9 + nx0.3 μs	1.7 + nx0.3 μs
SRC	Right Circular Shift	T8	1.8 + nx0.3 μs	1.6 + nx0.3 μs
SLN	Left Shift and Normalize	T8	4.2 + nx0.5 μs	4.0 + nx0.5 μs
SRN	Right Shift and Normalize	T8	4.1 + nx0.5 μs	3.9 + nx0.5 μs
DLA	Double Left Arith Shift	T8	3.1 + nx0.3 μs	3.0 + nx0.3 μs
DRA	Double Right Arith Shift	T8	3.1 + nx0.3 μs	3.0 + nx0.3 μs
DLL	Double Left Log. Shift	T8	2.4 + nx0.3 μs	2.2 + nx0.3 μs
DRL	Double Right Log. Shift	T8	2.4 + nx0.3 μs	2.2 + nx0.3 μs
DLC	Double Left Circular Shift	T8	2.4 + nx0.3 μs	2.2 + nx0.3 μs
DRC	Double Right Circ. Shift	T8	2.4 + nx0.3 μs	2.2 + nx0.3 μs
DLN	Double Left and Norm Shift	T8	4.5 + nx0.5 μs	4.3 + nx0.5 μs
DRN	Double Right and Norm Shift	T8	4.9 + nx0.5 μs	4.7 + nx0.5 μs
Control Instructions				
ENB	Enable	T8	3.5 μs	3.4 μs
HLT	Halt	T8	1.7 μs	1.6 μs
RIT	Reset Internal Interrupt	T8	1.7 μs	1.6 μs

		Addressing types	Execution times in μs	
			1.2 μs memory	0.7 μs memory
INH	Inhibit Interrupt	T8	1.7 μs	1.6 μs
LKM	Link To Monitor	T8	3.5 μs	3.4 μs
SMD	Set Mode	T8	1.7 μs	1.6 μs
Input/Output Instructions				
CIO	Control Input/Output	T8	4.4 μs	4.3 μs
INR	Input to Register	T8	5.3 μs	5.2 μs
OTR	Output from Register	T8	4.4 μs	4.3 μs
SST	Send Status	T8	5.3 μs	5.2 μs
TST	Test Status	T8	5.3 μs	5.2 μs
External Transfer Instructions				
WER	Write External Register	T8	4.6 μs	4.5 μs
RER	Read External Register	T8	5.1 μs	5.0 μs
TL	Segment Table Load (MMU)	T4 - T7	15.4 - 16.8 μs	12 - 13 μs
TLR	Segment Table Load Register (MMU)	T3	15.1 μ	11.7 μs
TS	Segment Table Store (MMU)	T4 - T7	15.4 - 16.8 μs	12 - 13 μs
TSR	Segment Table Store Register (MMU)	T3	15.1 μs	11.7 μs
FLD	Floating Point Load	T4-T7		4.4 - 5.3 µ
FLDR	Floating Point Load/Register	T3		4.1 µs
FST	Floating Point Store	T4-T7		3.7 - 4.6 µs
FSTR	Floating Point Store/Register	T3		3.4 µs
Move Table Instructions				
MVF	Move Table Forward (P857 standard)	T8	4.7 + nx2 μs	4.5 + nx1.8 μs
MVB	Move Table Backward (P857 standard)	T8	4.3 + nx2 μs	4.1 + nx1.8 μs
MVUS	Move Table from User to System (MMU)	T8	4.3 + nx2 μs	4.1 + nx1.8 μs
MVSU	Move Table from System to User (MMU)	T8	4.7 + nx2 μs	4.5 + nx1.8 μs

8 Data Flow and Control

The control of data flow within the system is governed by the action which is being carried out at the time. The main sources of control being the instruction set, the input/output processors, the interrupt system, and the bus control system. Data flow within the system is carried out via the general purpose bus. The input/output processors use conventional control circuitry whilst the control exercised by the instruction set, the interrupt system and the bus controller are via a microprogram held permanently within the control ROM of the CPU.

The following examples of data flow cover only the instruction set. The data flow and control of the input/output processors is covered later in chapter 10. As all the instructions are controlled in a generally similar manner only one instruction, an add instruction, is shown.

Figures 8.1 and 8.2 show a flowchart of the microprogram actions carried out during an add instruction which places the result in a register. The required microprogram instruction words would be accessed in sequence from the address generated by the ROM address generator. Three separate actions take place to carry out the complete operation:

1. The instruction is accessed from memory using the address in S REG and P REG are then incremented by 2 in preparation for the next action.
2. The method of forming the operand is decided. The operand is accessed and placed into REG M and Q.
3. The arithmetic action is carried out and the result placed into the specified register. The Condition Register is updated.
   At the same time the next instruction is fetched and the registers P and S are incremented by 2.

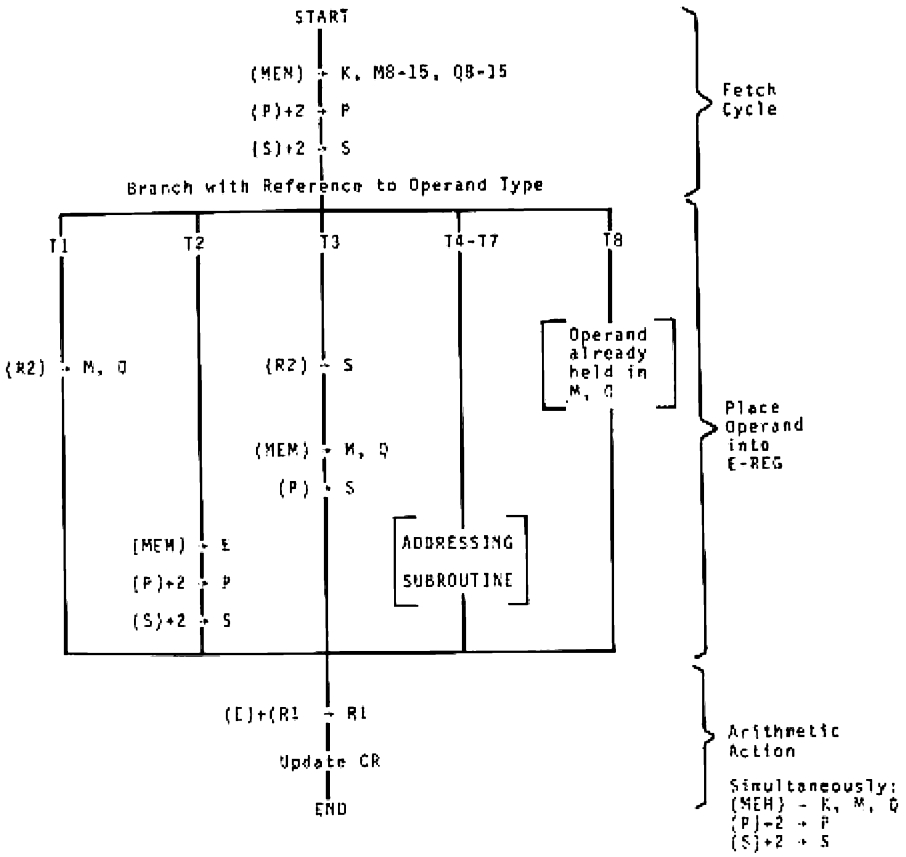


Figure 8.1 Instruction Microprogram

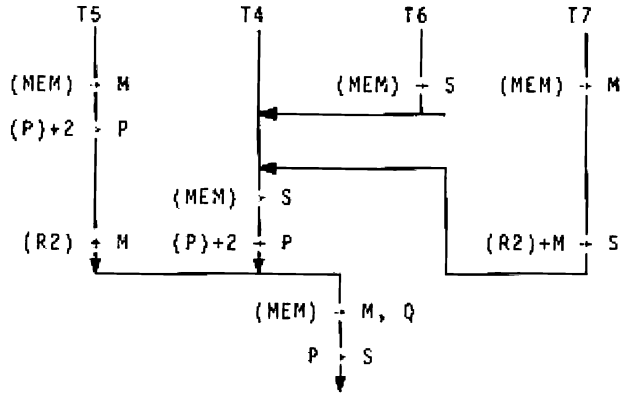


Figure 8.2 Microprogram Addressing Routine

Figures 8.3 to 8.6 show dia- ımatically the data flow involved in the basic arithmetic operations, with r- ect to the overall system block diagram on page 2-3.

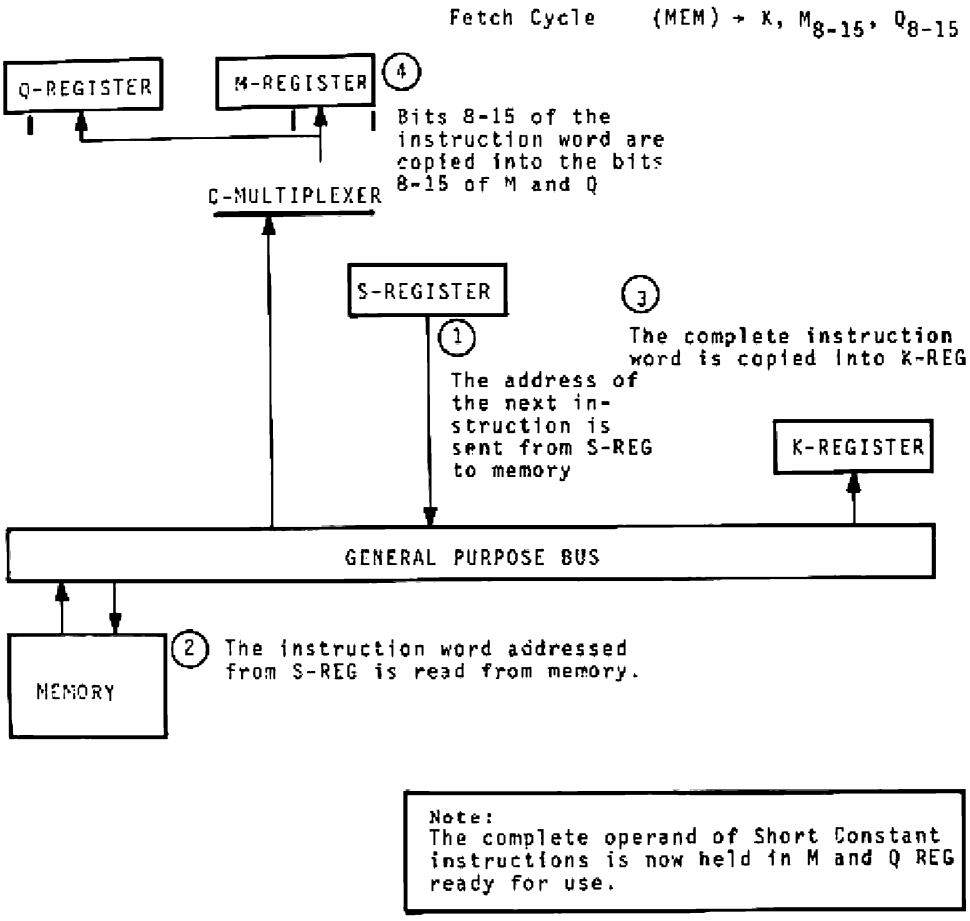


Figure 8.3 Accessing an Instruction

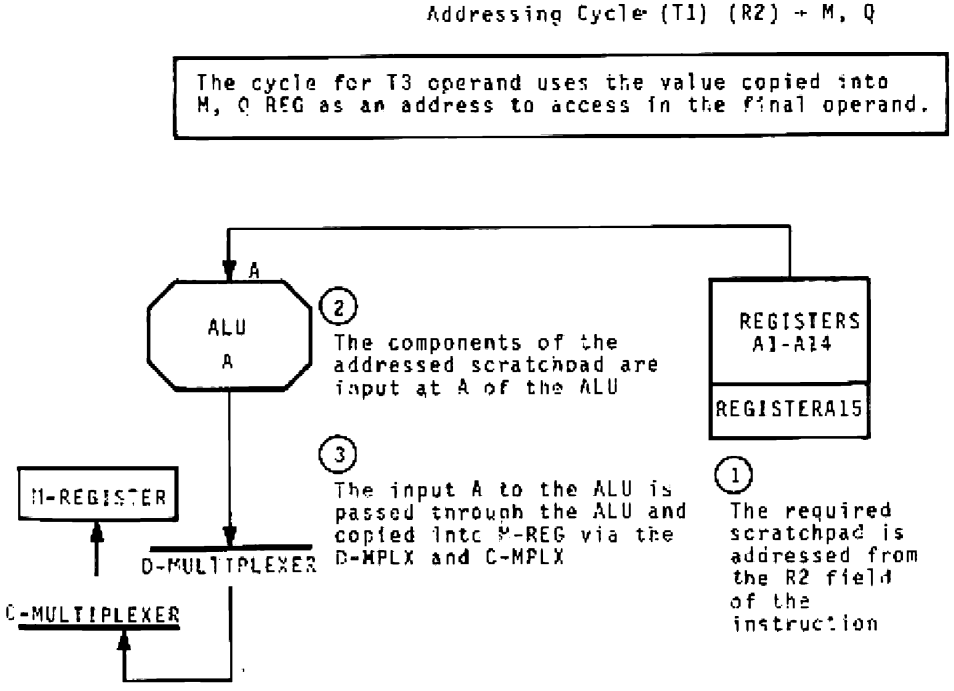


Figure 8.4 Addressing cycle (T1)

Addressing Cycle (T2 (MEM) → M, Q
(P)+2 → P
(S)+2 → S

Cycles for T4-T7 operands use the value initially copied into M-REG to compute the final operand address, using similar cycles.

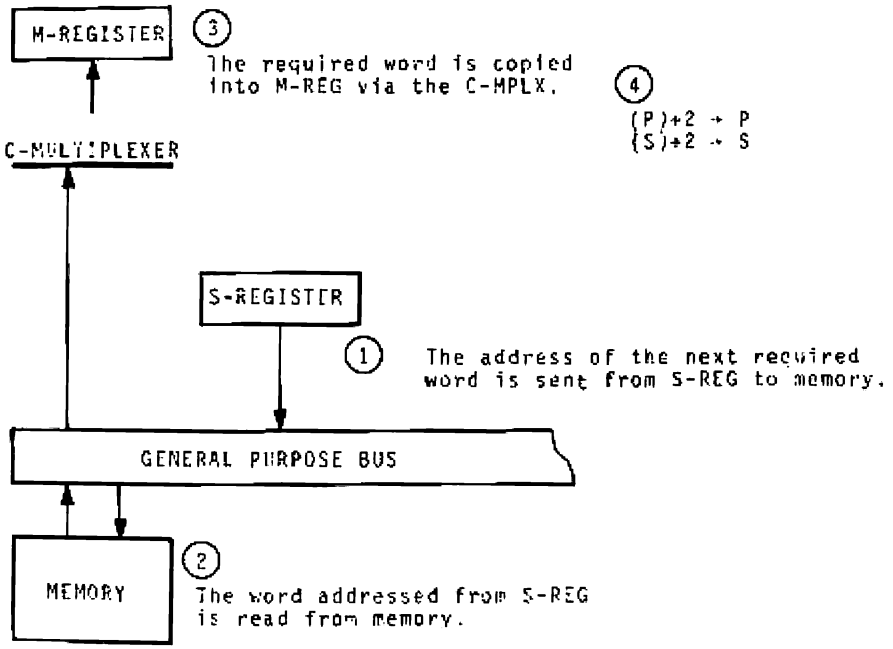


Figure 8.5 Addressing cycle (T2)

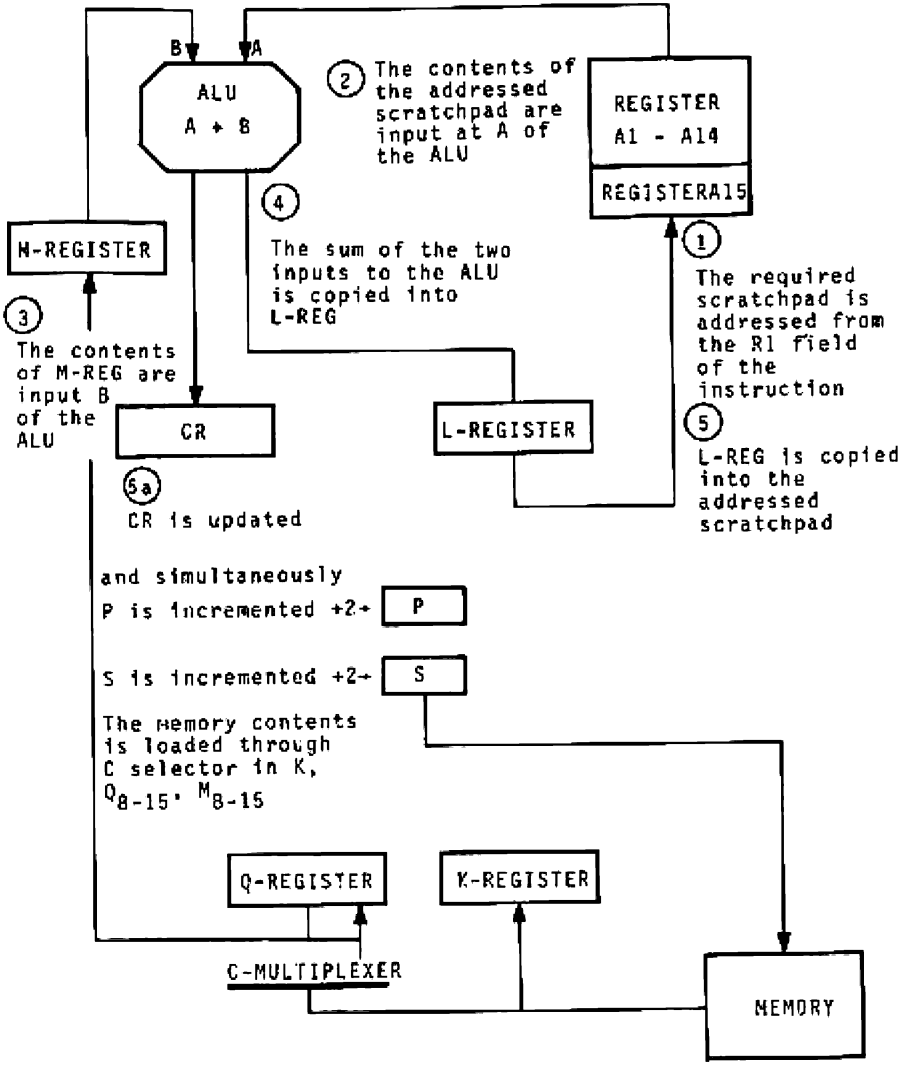


Figure 8.6 Execute cycle

The general purpose bus, consisting of 57 data, addressing, interrupt and control lines, handles the exchanges made between the main units of the system and for this purpose may be divided into four groups of signals each providing a separate bus function. The four function groups of the bus are:

1. Bus Control Functions
2. Data/Command Exchanges
3. Interrupt Handling Functions
4. Miscellaneous Functions

In order to gain the maximum efficiency from the bus certain of the bus functions may occur concurrently. Bus control functions may occur during the current data or command exchange, interrupt handling is carried out entirely independant of other facilities once it has been initiated, and miscellaneous functions may occur at any time and without reference to any other bus function.

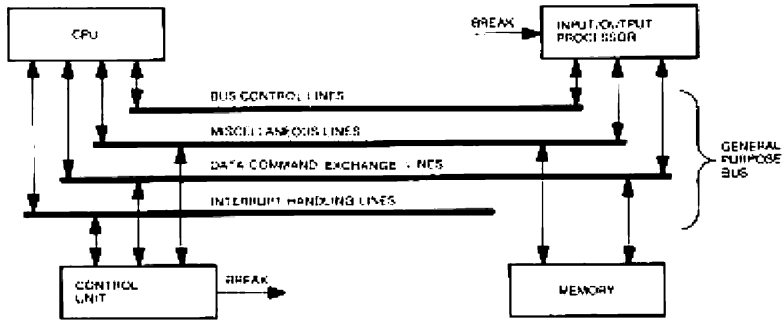


Figure 9.1 Connection of Standard Units to the Bus

BUS CONTROL FUNCTIONS

Efficient use of the bus for data or command exchanges is organized by a bus controller within the CPU. This controller allocates bus cycles for data or command exchanges one at a time, on a priority basis, to units which are able to request such cycles.

All units connected to the bus are known as master or slave units, and masters may act as either a master or slave depending on the type of exchange to be carried out. Units known as masters are those units which are capable of requesting a bus cycle for data or command exchanges and then, when the cycle is granted, controlling an exchange with either another master or slave, or controlling an exchange between two separate slaves. Units known as slave units are not able to request such bus cycles. To overcome clash conditions which may occur when two or more masters request a cycle simultaneously, normal bus allocations are made on a hardware wired priority basis to the masters, selection of the next master being carried out during the current exchange. Apart from this priority system the bus is allocated directly to the CPU in the event of a power failure being detected.

Priority Chain

The priority chain is hardware wired at installation time and within a standard system the CPU is given the lowest priority in the chain, other masters, such as the input/output processors will be given priority according to the system's requirements. Once a bus request has been made the bus controller initiates a master selection cycle to determine the highest priority master requesting the bus for a data or command exchange, as any number of masters may make a request at the same time. In response to a request a scan signal is initiated and is routed to all masters, via the masters, and in strict order of priority. The signal is only retransmitted from a master if the master is not requesting a bus cycle. In this way the highest priority master requesting a bus cycle is found and this master then indicates to all other masters that it has been selected. Any other lower priority masters that are requesting bus cycles remove their requests and must wait until bus requests are allowed before raising their requests again. The complete selection may take place during the current bus exchange cycle, whilst the bus is effectively busy, thus keeping the overall bus cycle time down to the time required for an exchange.

Figure 9.2 Shows a block diagram of the bus priority and selection system.

After being selected as the next master a master must wait until the exchange paths within the bus are no longer used. When this occurs the master takes control of the bus exchange paths, and removes its master selected signal from the bus. This final action allows a new master selection cycle to be carried out whilst the exchange cycle takes place.

DATA OR COMMAND EXCHANGES

These exchanges comprise data transfers with memory, command and response transfers to control units, and transfers with external registers.

As has been previously mentioned, before any such data or command exchange

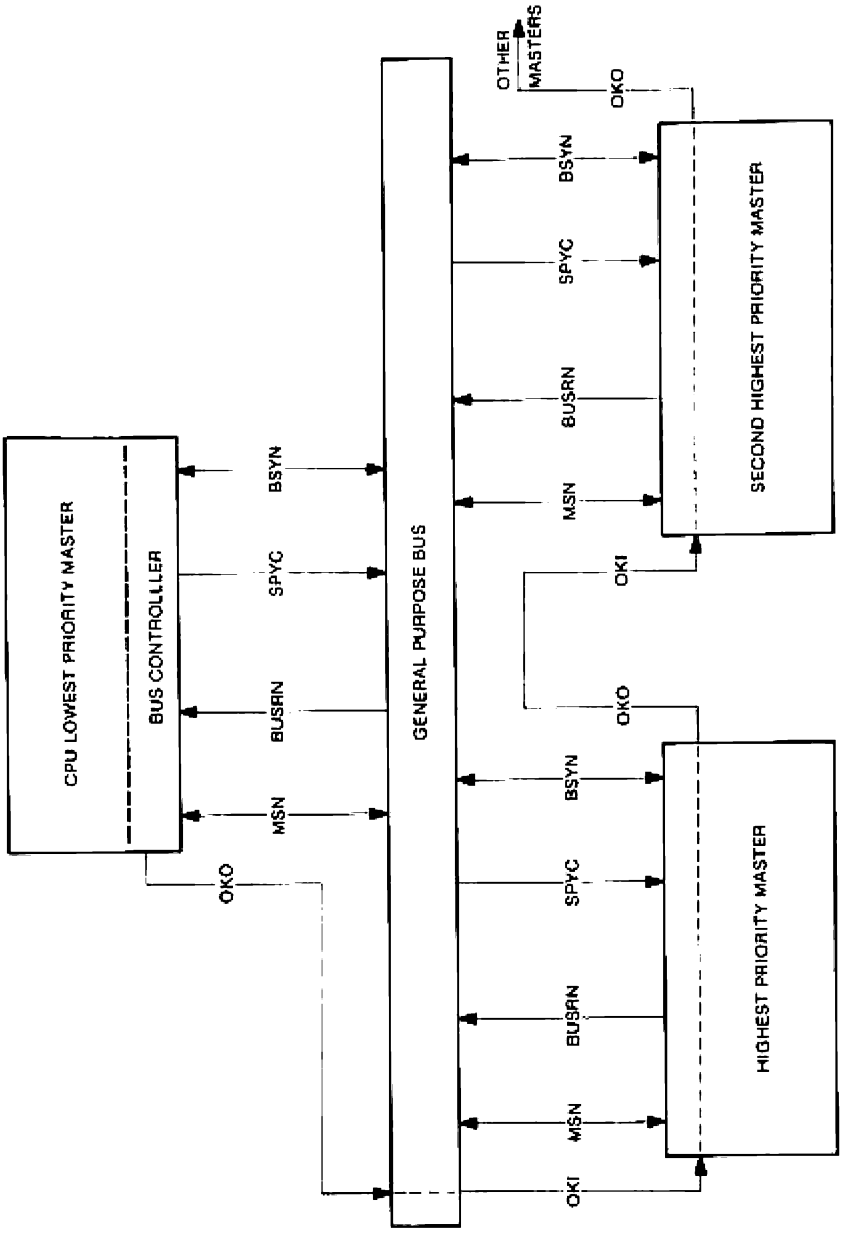


Figure 9.2 Bus Priority and Selection System

may take place, a master unit must request and be granted a data or command exchange cycle, and must wait until the previous data or command exchange has been completed before commencing its own exchange. Basically two types of exchange are possible:

1. Exchanges between the controlling master and another unit, where the other unit is either a slave unit or a master acting as a slave. e.g. CPU to Control Unit or CPU to I/O Processor.
2. Exchanges between two slave units under the control of a master, e.g. I/O Processor controlling an exchange between a CU and Memory.

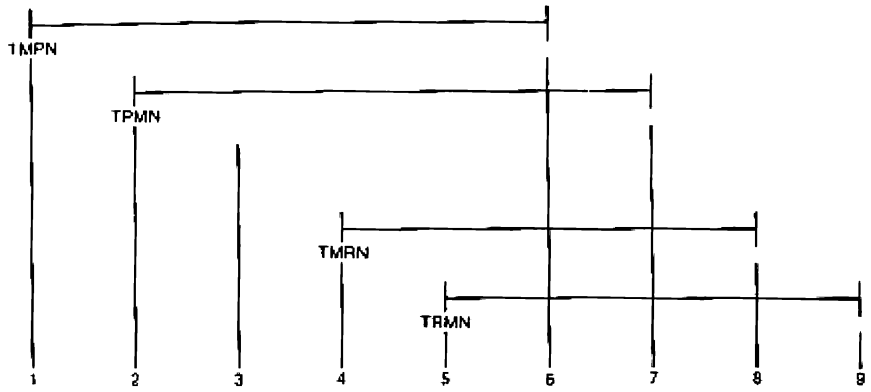


Figure 9.3 Exchange example

1 Control Unit Address and function set on the Bus and validated by TMPN
2 CU recognises address and accepts the function. Replies to master with TPMN
3 The master has now set up the CU and may now change the Address and Function, on the Bus.
CU remains set ready to receive data from the Bus
4 Memory Address and function set up on the Bus and validated by TMRN
5 Memory sets data on to the Bus and replies with TRMN
6 CU accepts data from the Bus TMPN removed
7 TPMN removed
8 TMRN removed
9 TRMN removed

Timing Control

The overall timing of exchanges made between units connected to the bus will differ widely and in principle will depend upon the type of device, and to some extent the physical positioning of the units on the bus. Control during an exchange is exercised with reference to timing and response signals raised by the units making the exchange and where necessary timing differences are accepted by the bus. This gives the system the ability to use either standard or non-standard peripheral devices without the need for special timing circuits, provided that the devices meet the overall requirements of the bus. In addition the bus includes a time out facility to unblock the priority system should for any reason a device or unit not reply to a timing signal from a master within 6.4 μs. In such a case the proposed exchange is aborted and the next selected master is allowed to commence its exchange. Figure 9.3 shows a simplified diagram of an exchange between a control unit and memory, under the control of a separate master (input/output processor). The timing signals used during the exchange are described later in this chapter and are shown as an indication of relative timing only, they are not to scale. Complete timing details of all transfers are available in the P856M/P857M Interface Manual.

INTERRUPT HANDLING

Interrupt handling is carried out independantly of other bus functions using separate bus interrupt lines, the CPU initiating a scan of the interrupt lines at the beginning of every instruction if the previous scanning took place at least 2 μs earlier. The operation of the overall interrupt system including the interrupt handling function of the bus is covered in the following chapter.

MISCELLANEOUS FUNCTIONS

These functions operate independantly of other bus functions and are concerned with the general reset and power on sequence within the system.

BUS SIGNAL LINES

The signals and lines associated with the four bus functions, N stands for active low, are:

Bus Control Signals

BUSRN *Bus Request*

The signal is raised by a master whenever it requires a bus data or command exchange cycle and bus requests are allowed.

SPYC *Scan Priority Chain*

This signal is raised by the bus controller in reply to BUSRN and indicates to all masters the commencement of a master selection cycle.

OKO/OKI — *Check Requests*

This signal is generated as OKO (OUTPUT) by the bus controller and received by the highest priority master as OKI (INPUT). It is chained through all the masters in order of priority as OKO/OKI. Onward transmission of the signal is inhibited by the first master which receives the signal and is requesting a bus cycle, this master is then selected as the next master.

MSN — *Master Selected*

This signal is raised by a master which has been selected as the next master to indicate the selection to all other masters. It is removed once the master concerned commences its exchange cycle.

BSYN — *Bus Busy*

This signal is raised by the master which has been selected and is now carrying out an exchange cycle. It is removed on completion of the cycle to allow the next selected master to commence its exchange.

Data or Command Exchange Signals

Timing Signals

TMRN — *Timing Master to Memory*

This signal is raised by a master and is used to validate the data and address, and to control the timing of an exchange with memory.

TMPN — *Timing Master to Peripheral*

This signal is raised by a master and is used to validate the control data and address, and to control the timing of an exchange with a peripheral control unit.

TMEN — *Timing Master to External Register*

This signal is raised by a master and is used to validate the data and address, and to control the timing of an exchange between a master and a unit containing an external register.

TRMN — *Timing Register/Memory to Master*

This signal is raised by memory or a unit controlling a register. It is used together with signals TMEN and TMRN in the controlling of an exchange cycle with a register or memory.

TPMN — *Timing Peripheral to Master*

This signal is raised by a peripheral device control unit and is used together with signal TMPN in the controlling of an exchange cycle with a peripheral device's control unit.

Bus Address Lines

MAD128, MAD64, MAD00 to MAD15 *18 Address Lines*

These lines carry the memory address, register address, or peripheral address and requested function, during any exchange and are qualified by the timing signals from a master:

1. Memory Exchanges (Qualified by TMRN)
   MAD00 to MAD14 – These lines carry the 15-bit memory address required to access up to 32k of memory.
   MAD15 – This line is only significant in character operations and is used to define the character within the addressed word which is to be used.
   MAD64, MAD128 – These lines enable the extension of memory addressing to 64k and 128k words.

2. External Register Exchanges (Qualified by TMEN)
   MAD08 to MAD15 – These lines carry the 8-bit register address required to access up to 256 registers.
   MAD04 – This line is used to indicate a read or write operation to the addressed register.

3. Peripheral Control Unit Exchanges (Qualified by TMPN)
   MAD10 to MAD15 – These lines carry the 6-bit device address required to access up to 64 control units.
   MAD04 – This line is a function line used to indicate the direction of the exchange.
   MAD08 – This line is a function line used to indicate whether the exchange is a data exchange or a command or status exchange.
   MAD09 – This line is a function line reserved for use by special functions.
   MAD03 – This line is used to indicate whether the current word or character exchange is the last when exchanges are organized in blocks.

Bus Data Lines

BIO 00N to BIO 15N *Input/Output Lines*

These lines are the 16 input/output lines used to carry data between the units making an exchange.

ACN *Accept*

This signal is sent from a control unit to indicate that it accepts the request to carry out a designated function.

WRITE *Write*

This signal is raised by a master controlling an exchange with memory to indicate that the exchange is a write to memory. When the signal is not present a read from memory cycle is indicated.

CHA *Character*
This signal is sent from a master to memory to indicate that the requested exchange is to be carried out in character mode.

Bus Interrupt Lines

SCEIN *Scan External Interrupts*
This line is used to allow units connected to the interrupt system via the bus to raise the bus interrupt lines as required.

BIEC *Bus Interrupt Encode*
These lines are the 6 lines which carry the encoded value, 0 to 62, of the highest priority outstanding interrupt request to the interrupt system.

Miscellaneous Signals

CLEARN *Clear*
This signal is sent from the CPU to all units connected to the bus and initiates a general reset of all such units.

RSLN *Reset Line*
This signal is raised during the power on or power restoration sequence and is used within the system to ensure an orderly commencement or resumption of operation without loss of data.

PWFN *Power Failure*
This signal is raised during the power off or power failure sequence and is used within the system to ensure an orderly run down of operation without loss of data.

The interrupt system within the CPU enables both internal and external interrupts to indicate that certain action is required with reference to the interrupt. This indication is given by raising an interrupt signal. Efficient handling of these interrupt signals is carried out by the hardware in conjunction with the system's software, ensuring that interrupts are serviced in the correct order of priority and with complete recovery facilities to the original program once the interrupt has been serviced.

ORGANIZATION

Within any system 63 individual interrupt signals are possible to control the priority running of 64 levels of program. Interrupt priority levels are numbered and encoded from 0 to 62, level 0 being given the highest priority. Signals at interrupt levels 0 to 7 are directly connected to the interrupt system at the CPU and are not encoded in binary form on the interrupt lines of the general purpose bus. Certain of the lines 0-7 are used by internal interrupts from the system and such lines are therefore reserved, the remaining lines in the group 0-7 may be used by facilities which are fitted within the basic mounting box. Signals at interrupt levels 8 to 62 are always encoded as a 6-bit binary value corresponding to their level and connected to the interrupt system via the interrupt lines of the general purpose bus.

OPERATION OF THE PRIORITY SYSTEM

Control units have priority levels set by hardware wiring within themselves and raise the required 6-bit value directly when an interrupt is raised. Two separate types of interrupt action may take place, one handling the eight possible interrupt signals which are directly wired within the CPU and the other handling all interrupt signals received via the general purpose bus.

The 8 basic interrupt signals are connected to their own priority encoder, the 3 output lines of which are connected via multiplexer to the system comparator. The multiplexer also accepts the encoded signals from the interrupt lines of the general purpose bus but is wired to give priority to the basic interrupt signals. The system's comparator compares the value presented by the multiplexer with the value already held within the PL register. Only of the value from the multiplexer is lower, that is higher in priority, than the value in the PL register

is further interrupt action taken. Once an interrupt of higher priority than the running program is detected a check is made to see if interrupts are allowed, the instructions ENB and INH being used to control such enabling.

Note: The connection of the magnetic tape control unit to the system requires an additional bus and translator board. The interrupt signal of this control unit is wired in a slightly different way. Refer to the Interface Manual for more details.

INTERRUPT ACTION

Interrupt action is carried out in two distinct parts:

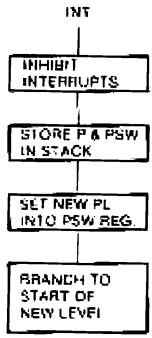
1. The initial hardware action.
2. The programmed software action.

Together these actions must ensure that the correct level of program is entered, and that sufficient information with respect to the interrupted level is kept safely so as to enable this level to be restarted correctly once the interrupt has been dealt with.

Associated with the hardware action is a fixed and reserved word in memory for each of the levels, locations /0 - /7C being used for levels 0 - 62 respectively. These locations, referred to as hardware interrupt locations, are addressed from a decode of the priority levels given to the interrupt lines and should always contain the start address of the associated level's coding. Start addresses for all the levels to be used in any program must be decided upon by the programmer and then set into the correct hardware interrupt locations by either the loading process, or by the initial running of the program.

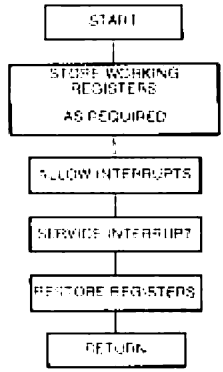
The following flowcharts and explanations cover the hardware and software actions of the interrupt system and assume that interrupts are allowed and that the stack is empty at the commencement of the actions.

1. Hardware interrupt action commences by inhibiting further interrupts thus allowing the present to be serviced without interference if this is necessary.
2. The contents of the P and PSW registers are stored in a memory stack addressed from register A15. Hardware updating of register A15 is carried out each time a word is stacked.
3. On completion of the stacking operation the priority level of the interrupt is set into the PSW register, overwriting the original contents.



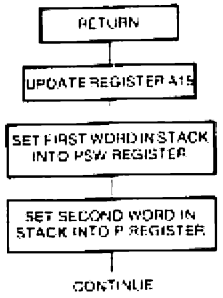
4. A branch is now made to the start of the new level's coding. This is carried out by using the priority level of the interrupt to address the required hardware interrupt location, the value in the addressed location is then set into the P register and is the address at which the program restarts after hardware interrupt action.

At this point the P and PSW registers contain information which is relative to the new level of program, the address at which the interrupted level is to restart and the PSW for this level. Further interrupts are inhibited. Instructions are now carried out from the new program level and it is these instructions which service the interrupt and define the software interrupt action to be taken, (usually an INR, OTR, SST, CIO Halt or an RIT instruction).



1. It may be required that the content of working registers being used by the interrupted level need to be stored. If this is required then the system stack may be used for this purpose and the contents of the registers will be stored consecutively with the contents of the P and PSW registers of the interrupted level. Alternatively a separate safe area may be designated and used for the preservation of the working register's contents.
2. Interrupts from higher levels may of course occur at any time and it may be required that these are serviced. If this is the case then interrupts may be allowed before any action to store the working registers, and in this case the higher interrupting level should store the contents of the working registers it intends to use. The order in which storing of registers and the enabling of interrupts is carried out is a matter for the programmer to decide with reference to the specific requirements of the overall program.
3. Whichever action or device caused the interrupt may now be serviced and any necessary program flags or switches must be set before completing the routine.
4. Before a return is made to the originally interrupted level any working registers which were saved must be restored correctly either from the system stack or from the specific safe area used.

At this point the required action of the interrupt routine is complete, all necessary flags and switches are set, and the working registers contain the values required by the originally interrupted level. The PSW and P register values required by the original level are addressed by register A15. Return action may now be requested using the Return instruction and specifying register A15 as the stack pointer within this instruction.



1. The contents of register A15 are updated to address the first word of the stack as it stands. The PSW and P registers still contain the original level.
2. The first word of the stack is set into the PSW register, restoring the original level's PSW.
3. The second word of the stack is set into the P register, thus specifying a branch to continue the original level when program action is resumed.

Before program action is resumed any outstanding interrupts are checked for priority against the value in the PL part of the PSW register. If a higher level interrupt exists then this is serviced in the manner just explained. If no higher level interrupt exists then the original level continues.

Figure 10.1 shows diagramatically a possible interrupt sequence.

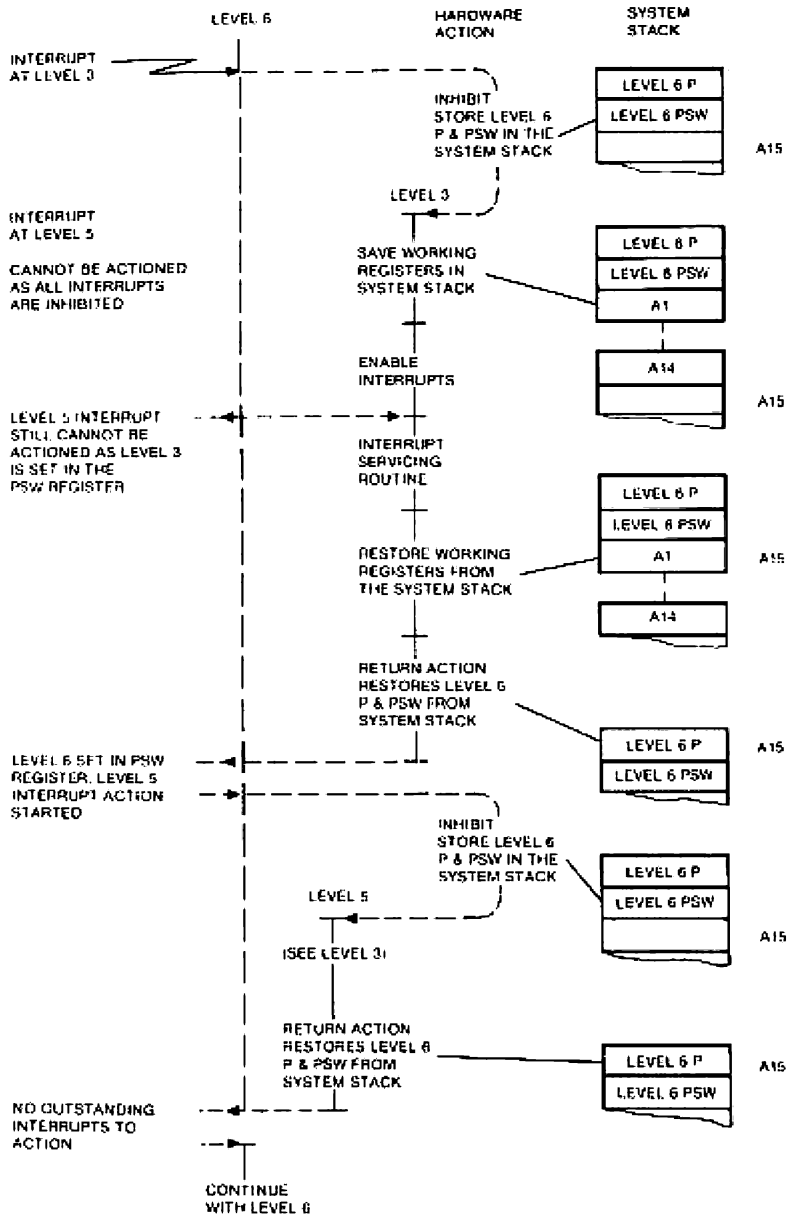


Figure 10.1 Diagram of interrupt sequence

STACKING

The use of register A15 as a stack pointer gives the user the facility of automatic updating of this register. Updating is carried out each time A15 is used for addressing purposes by decrementing its contents by 2, thus the stack is filled from the higher addressed locations to the lower addressed locations. The programmer is responsible for determining the size of the stack required and for setting the start address of the stack into register A15. A further facility available to stack handling is the generation of an interrupt when the stack pointer address is <128, this enables action to be taken to ensure that the stack does not overwrite any of the reserved area at the beginning of memory.

Data transfers within the system may take place between any unit which is destinated a master and another master or slave unit, or between two slave units under the control of a master. All data transfers take place via the general purpose bus and within the system take the form of parallel 16-bit word, or 8-bit character transfers. Figure 11.1 shows a diagramatic layout of the units concerned with data transfers and the channels with which each is associated. The exchange paths available within the system are:

- CPU/Control Unit
- CPU/External Register
- Memory Slave
- Memory Master

The basic transfer channel is the programmed channel which uses only the CPU/Control Unit path to transfer data, one character or word at a time, between a CPU register and a control unit. Optionally available within the standard system are the input/output processor channels. These channels may be used by devices connected directly to the general purpose bus and may use the same control units which are used for connection to the programmed channel. Up to 64 input/output processor subchannels may be connected and used simultaneously via a priority system of servicing exchange requests. Priority allocations being made initially to an input/output processor as a master, and secondly to one of the subchannels available within each processor. Transfers carried out via the input/output processor channels use three of the exchange paths:

- CPU/External Register to set up the transfer parameters
- CPU/Control Unit to start or stop the transfer and check the status of a device as necessary.
- Memory/Slave to allow the direct transfer of data between the memory and the control unit as initiated by the input/output processor.

In addition to these channels, two non standard modes of operation are possible, each using one of the available exchange paths. Direct access to memory is possible using the Memory/Master path and transfers between internal and external registers are possible using the CPU/External Register path.

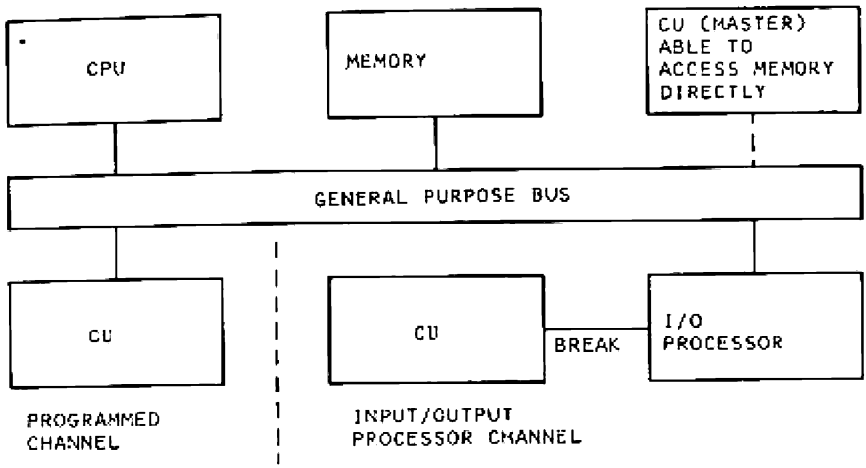


Figure 11.1 Units concerned with transfers

CONTROL UNITS

Details of the standard control units available within the system are given in chapter 16. A control unit is required to connect any external device to the system. The function of the control unit is to translate the address, control, and timing signals of the general purpose bus into the necessary signals to exercise discrete control of the device. The basic requirements of any control unit are:

1. Address Decoder
2. Function Decoder
3. Sequence Control - to enable the device to transmit and receive data and to control the initial starting and stopping of the device.

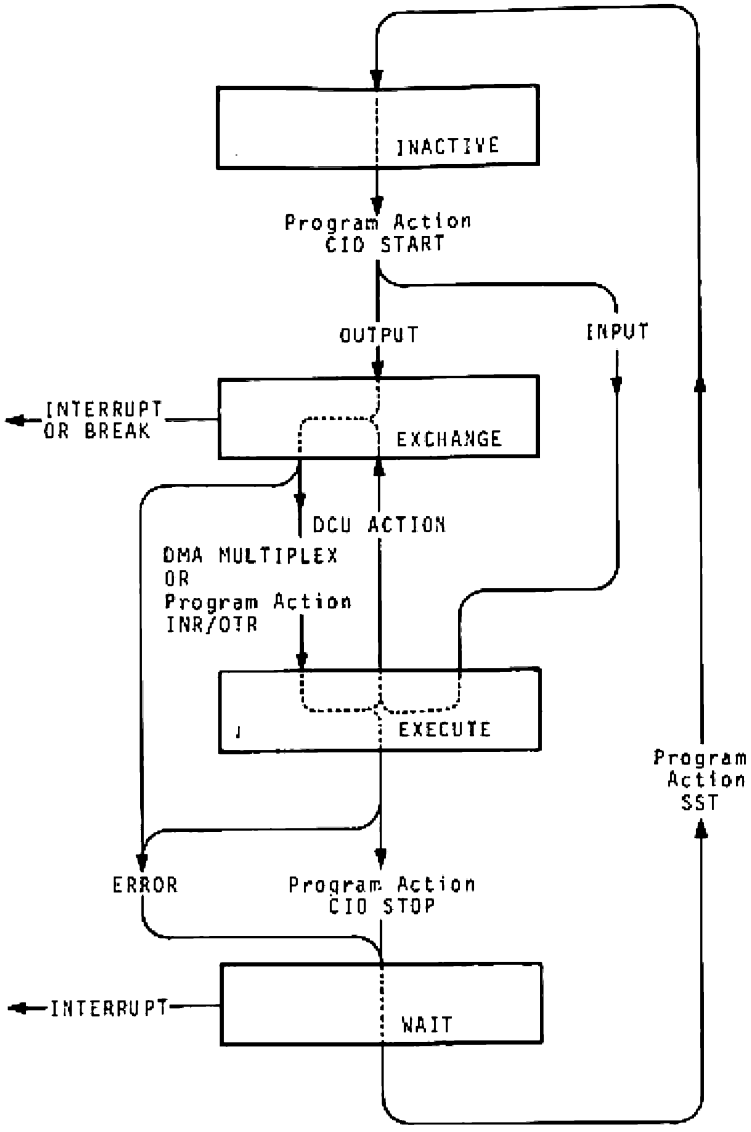


Figure 11.2 Four states of standard control unit

The standard control units used within this system are required to carry out four separate actions and have a state of operation associated with each of the actions, particular functions are carried out with respect to the commands received and the current state of the unit.

Figure 11.2 shows the four possible states of a standard control unit and indicates the actions necessary to change from one state to another.

The four states are:

1. *Inactive* In this state no exchange is possible. The control unit must be sent a start command before any transfer can take place.

2. *Exchange* In this state the control unit is waiting for a transfer to be initiated. The transfer may be input or output and must be intialized by a master unit. On completion of the exchange the control unit switches to the execute state.

3. *Execute* In this state the control unit carries out either an exchange with the device it is controlling, or any other command it has received. The action is carried out entirely independant of the remainder of the system and on completion the control unit switches to the exchange state.

4. *Wait State* This state is entered from the exchange or execute states when a stop command is received or on the occurrence of an error. In this state the control unit is waiting to send its status and will switch to the inactive state when it receives a request for status command.

Because all transfers are carried out via the general purpose bus on a priority basis all control units connected directly to the bus, whether for fast or slow devices, can use the same basic design and may be connected at a priority level in accordance with the remainder of the system. When connection is made via the input/output processors the break line from the unit is connected directly to the appropriate channel and not via the general purpose bus.

Control Units Connected Directly to the GP Bus
These control unit form their own encoded interrupt signals. Figure 10.3 shows an overall block of such a control unit and the signals associated with it.

DEFINITION OF UNITS

The definition of units as masters or slaves and the control exercised by masters within a standard system is:

CPU - Master

Normally given the lowest priority access to the bus, apart from specific cases. As a master it is able to control exchanges between itself and other masters or slaves.

Input/Output Processors - Master

As a master an input/output processor is normally given a priority in accordance with its importance within the system and is able to control exchanges between the memory and a device control unit, both of which will be designated slaves. Acting as a slave the input/output processors are initially set up by the CPU.

Memory - Slave

The memory is always a slave and is controlled during an exchange by a master.

Standard Device Control Units - Slave

Standard device control units are always slaves, and are controlled during an exchange by a master.

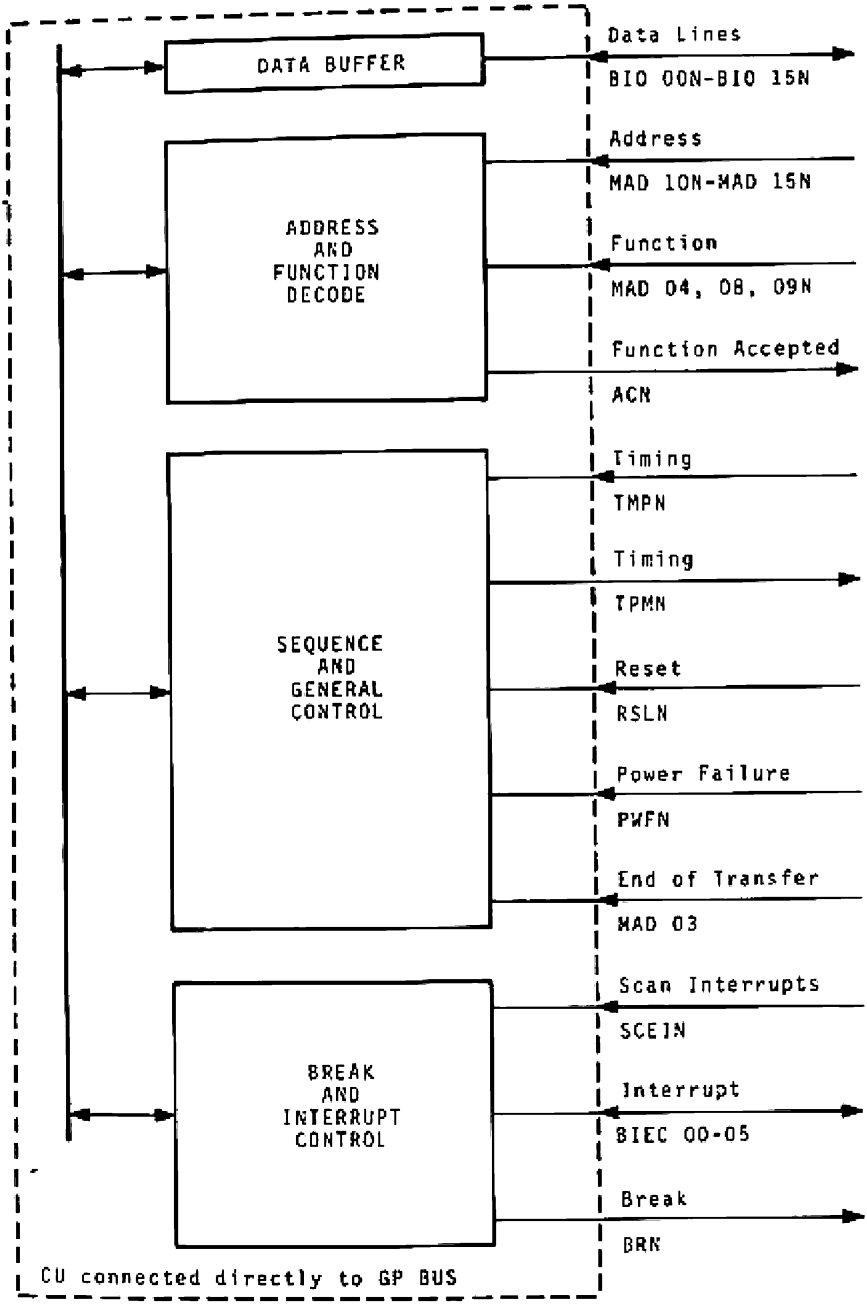


Figure 11.3 Signal Exchange

PROGRAMMED CHANNEL

The programmed channel is the basic transfer channel and is standard with all systems. Apart from providing an exchange facility between a control unit and the CPU, it also provides the initialization path between the CPU and the input/output processors. In all actions concerning the programmed channel the CPU is the controlling master.

Data are transferred by the use of specific input/output and external register instructions within a program and each word or character exchange requires a separate instruction. Apart from the instructions which carry out the exchanges, instructions are available to start and stop a device and to check the status of a device. In practice program loops are used in the control of a block transfer.

Two possible modes of operation exist when using the programmed channel for data transfers:

Wait Mode
This is the simplest but slowest form of transfer and is in most cases never used. Each word or character is exchanged separately and the complete program is held up in a waiting loop between individual exchanges. In this mode the maximum transfer rate obtainable is dependant on the time taken to execute the necessary program loop, or the time taken by the device concerned to execute a single exchange, whichever is the slowest.

Interrupt Mode
By the use of this mode, operation of the programmed channel is carried out without the use of time consuming waiting loops. Each word or character is still exchanged separately, but the necessary instructions form a part of an interrupt routine. This means that the main part of any overall program can continue to be executed during the time taken to actually carry out an exchange.

When the device control unit is ready to exchange another character it raises an interrupt and the main program is stopped whilst the new exchange is initiated by the interrupt routine. On completion of the interrupt routine the main program is restarted and continues whilst the exchange is in progress. This sequence can be continued until either the necessary transfer is complete or until the main program requires to use the transferred data. In the second case the main program must be made to wait as necessary.

Commands and Responses
To enable operation of a control unit via the programmed channel the following instructions may be used as commands to control units.

CIO START
CIO STOP
INR
OTR
SST
TST

The responses given to these commands are set into the condition register:

CR = 0 Command Accepted
CR = 1 Command Rejected
CR = 3 Address Unknown

The use of the External Register instructions used to initialize the input/output processors will be covered when the input/output processors are explained.

Control and Data Flow
As only one method of forming the operand for input/output instructions exists, T8 Short Constant, the control sequence for all instructions is similar, the main difference being between the input, INR, SST, TST instructions and output, OTR, CIO instructions. Figures 11.4 and 11.5 show diagramatically the data flow involved during the action of the input/output instructions.

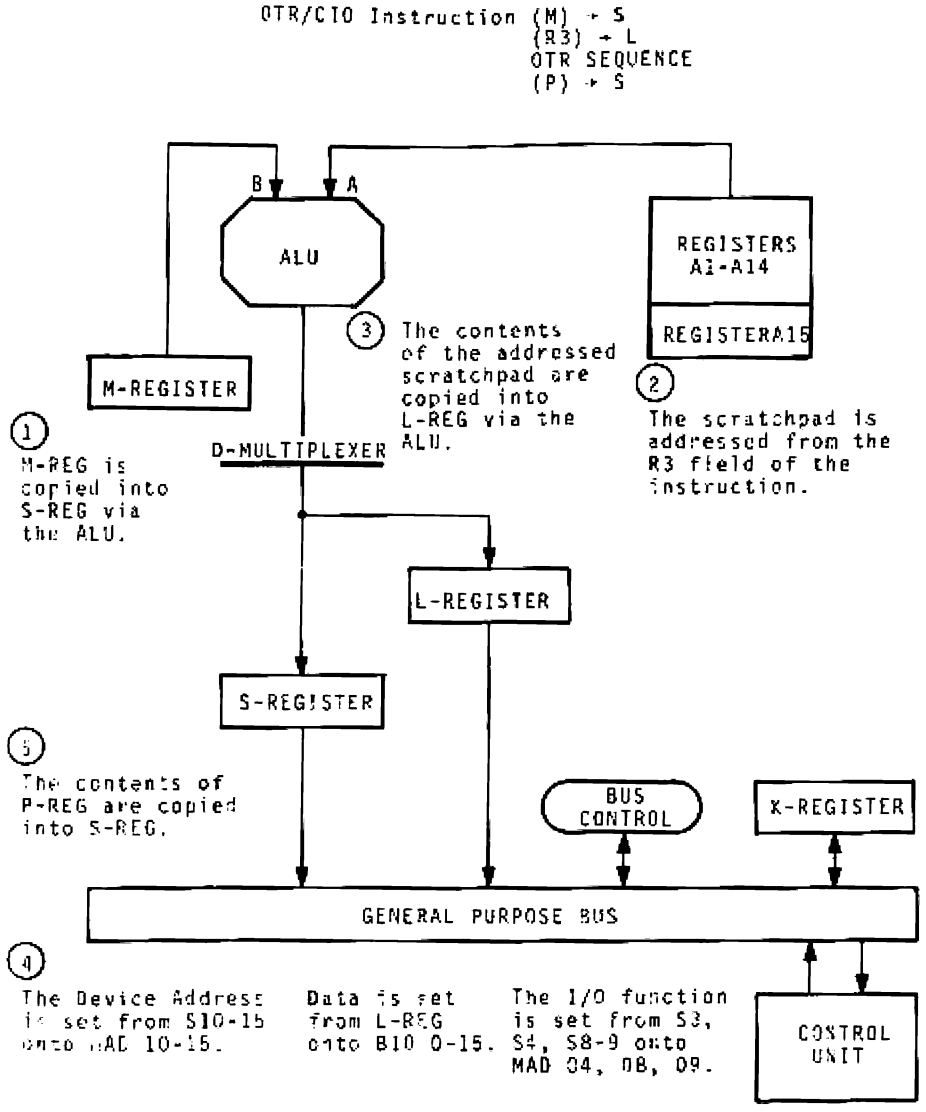


Figure 11.4 OTR/CIO Instructions Flow

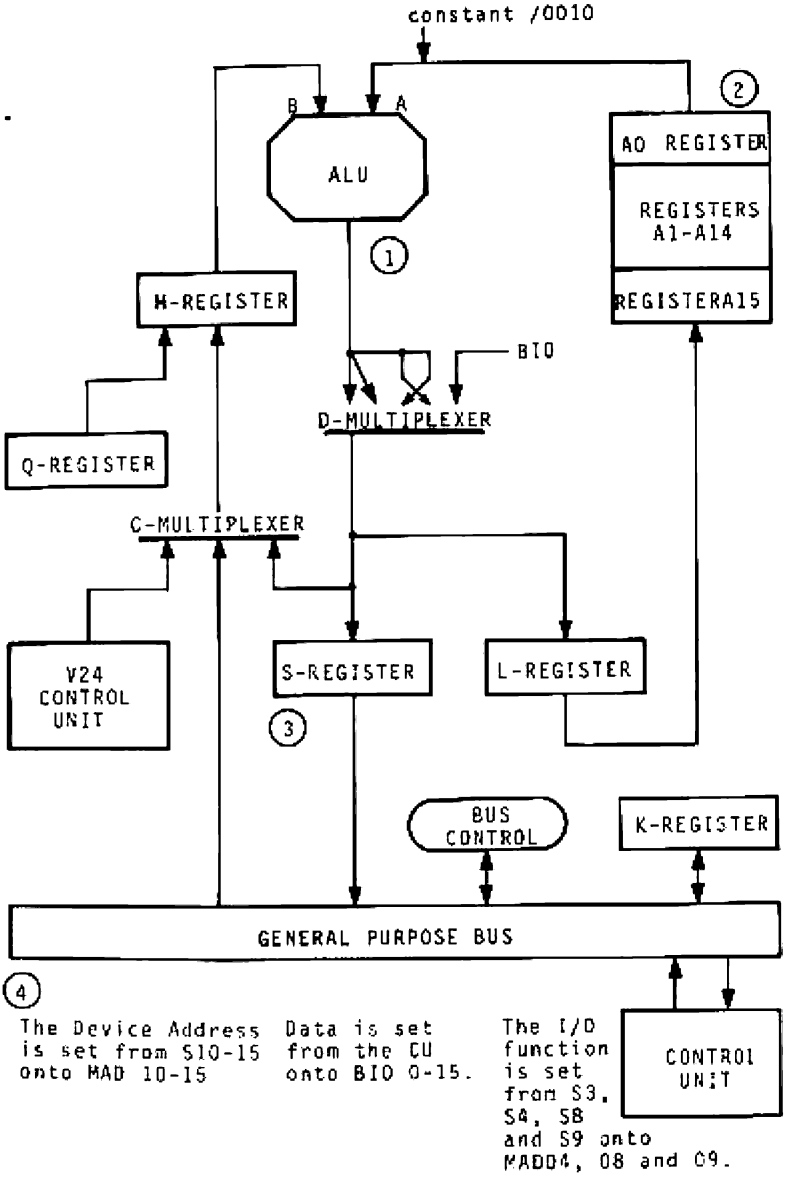


Figure 11.5 INR/SST/TST Instructions Flow

1 The constant /1000 is loaded in M (/10 on A input of ALU, D in exchange character mode, and C Multiplexer).

2 The constant /800 is loaded in AO through ALU, D in shift right mode, and L register. In the same time Q contents (0, K08-K15) is loaded in M.

3 The logical "or" of M and AO is loaded in S register. At the exchange time contents of S will be sent on MAD lines.

4 The exchange itself takes place - B10 are copied in R3 register through D and L and the output of the Serial Control Unit in M register - Then a logical "or" of R3 and M is returned to scratch pad R3.

INPUT/OUTPUT PROCESSOR CHANNELS

The input/output processor channels provide a fast method of block transfer between the system's memory and up to 64 different device control units. Transfer rates of up to 830k words/sec or 1.2Mw for the fast memory being possible. A maximum of 8 input/output processors is possible and each is capable of controlling up to 8 subchannels. These channels replace the normal instruction sequence of a programmed channel transfer with a hardware sequence to carry out each exchange, and a data path is provided between the appropriate device control unit and memory via the general purpose bus.

Both types of control unit available may be connected via the input/output processor channels and in all cases the control units may be addressed from either the appropriate input/output processor or from the CPU. The normal states and sequencing of the device control units apply but the interrupt raised in the exchange state for the programmed channel is replaced by a break signal wired directly to the input/output processor's priority system and used to initiate each hardware exchange sequence.

Organization
Any number of the devices connected to the input/output channels may be set up and started so that the overall transfers of each are carried out together. All break requests would be serviced according to a priority given to each device and derived in two separate ways:

1. Where more than one input/output processor is connected to the system each separate processor would have a priority according to its position in the chain of masters.
2. To enable each processor to differentiate between the 8 break signals from the possible 8 devices connected to it, the break lines are connected to the channels via a priority system.

Each time a break request is received by a channel, the channel requests a bus cycle. When the cycle is granted the channel carries out a single exchange between the device control unit having the highest priority break request outstanding, and the memory.

Associated with each of the possible 8 control units connected to any channel are two 16-bit registers which hold the parameters of any transfer to be carried out with a unit. Prior to any transfer the two registers must be correctly set up to hold the transfer parameters. During any transfer the registers are hardware addressed from the priority decoding of the break signals and are used and updated by the I/O processor.

Figure 11.6 shows the layout of the control registers, the contents of which are known as First Control Word and Second Control Word respectively.

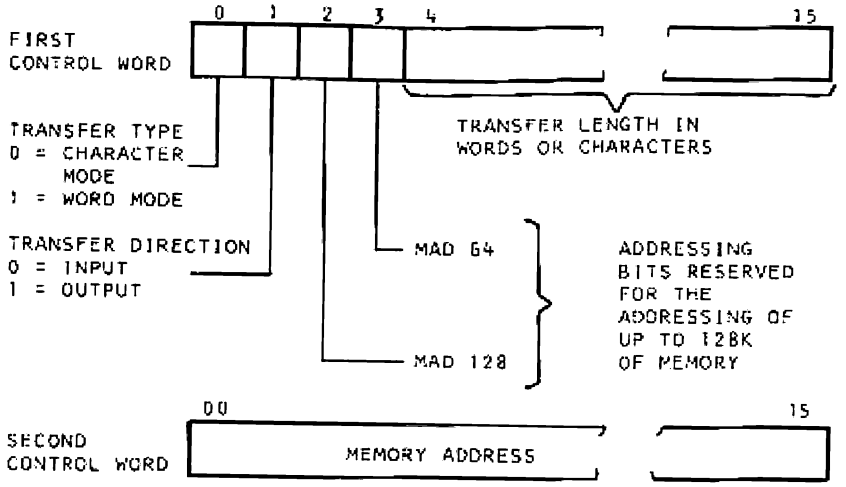


Figure 11.6 I/O Processor Control Words

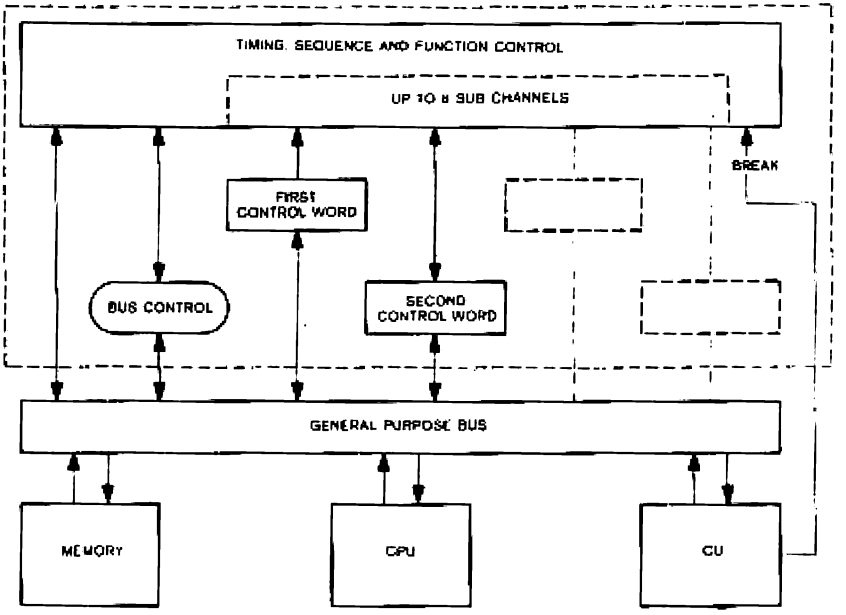


Figure 11.7 I/O Processor within the system

Control and Data Flow
Figure 11.7 shows a diagramatic layout of an input/output processor within the system.

Three separate control paths are used during an input/output processor transfer:

1. CPU to Input/Output Processor
When this path is in use the CPU is the master of the exchange and the input/output processor acts as a slave. The exchange takes place between the CPU and the input/output processor using Read or Write External Register Instructions. Write External Register instructions being used during the setting up of the processors and Read External Register instructions being used to read the contents of the control words during end or error routines.

The format of the Write External Register Instruction and the appropriate part of the data flow concerned when setting up the two control words are shows by figures 11.8 and 11.9.

Layout of Read/Write External Register Instruction.

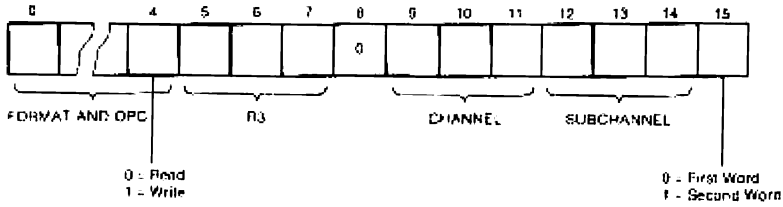


Figure 11.8 Read/Write External Register Layout.

R3 – The contents of R3 is the value which is to be set into the control word.

CHANNEL – The channel is the number given to a particular processor with respect to its priority relative to the possible 8 processors which may be connected to the system.

SUB CHANNEL – The subchannel is the priority given to a particular control unit relative to the possible 8 devices which may be connected to each channel.

The action of the instruction within the CPU is to copy bits 8-15 from K REG into S REG via M REG and copy the contents of R3 into L REG, before carrying out an OTR SEQUENCE. Note, bit 4 from the OPC is used to define the instructions as Read or Write.

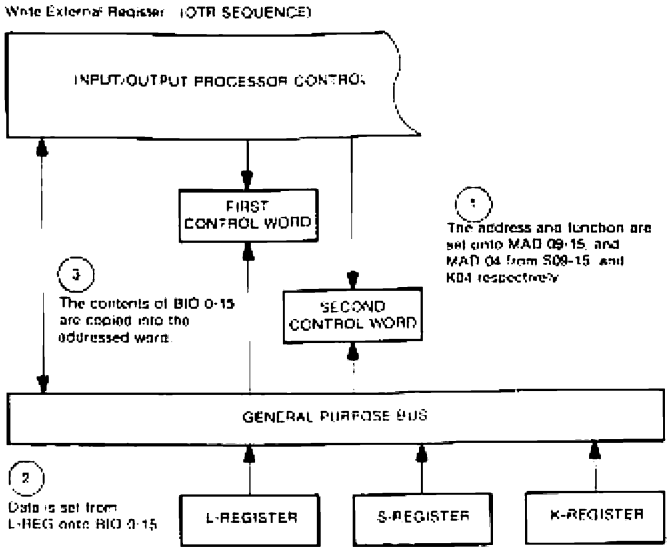


Figure 11.9 WER Instruction Flow

2. CPU to Control Unit

When this path is in use the CPU is the master of the exchange and the control unit is the slave. The exchange takes place between the CPU and the control unit, data flow being as for programmed channel transfers. (See figures 11.4 and 11.5). By the use of this path the devices connected to the input/output processor channels may be stopped and started, and their status requested.

3. Input/Output Processor to Memory and Control Unit

When this path is in use the input/output processor is the master of the exchange and the memory and control unit are slaves. The exchange takes place between the memory and the control unit. Figures 11.10 to 11.12 show an outline of the exchange action and the data flow during the two cycles which comprise an exchange.

Such an exchange would be initiated after the receipt of a break signal and after the input/output processor had requested and been granted a bus cycle. The break signal would be removed once the necessary actions to initiate an exchange had been carried out.

Note: A further exchange with respect to the overall transfer would be carried out immediately if the control unit raises its break line again, during the execution of the current exchange, and providing no other higher priority breaks or master requests are outstanding.

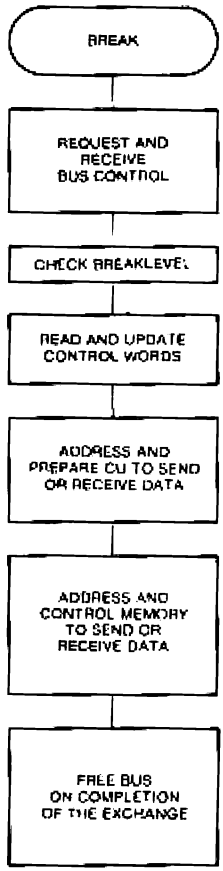


Figure 11.10 Exchange action

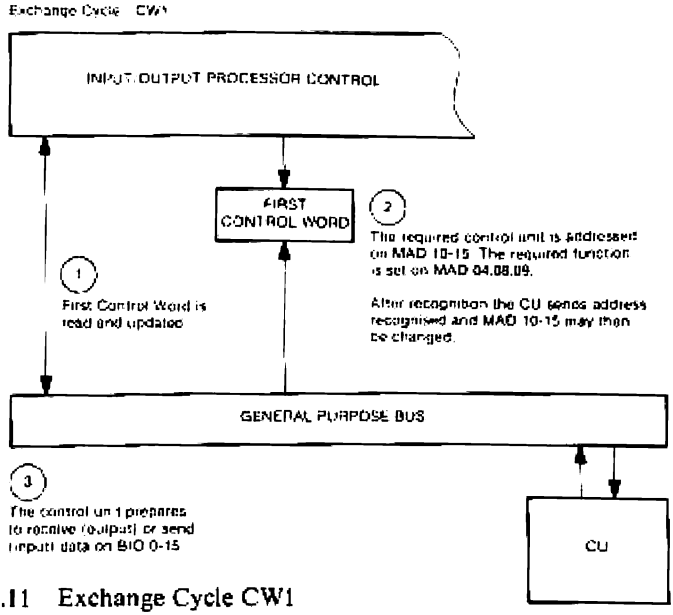


Figure 11.11 Exchange Cycle CW1

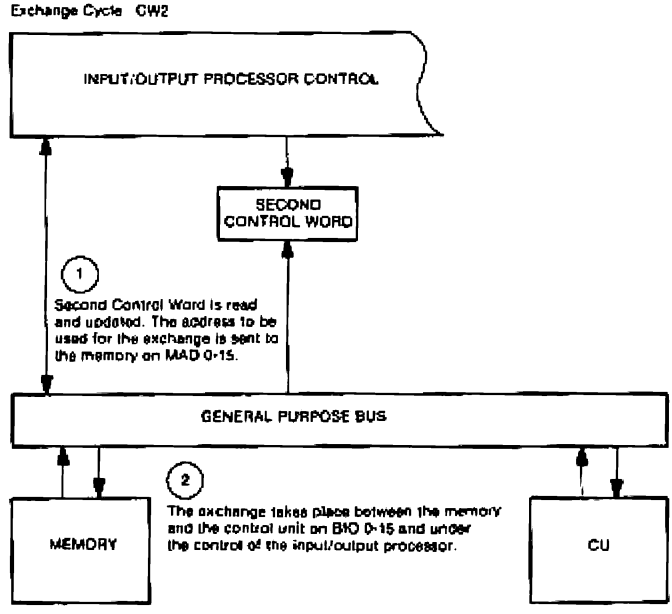


Figure 11.12 Exchange Cycle CW2

DIRECT MEMORY ACCESS

The Direct Memory Access channel manages data transfers directly between memory and a single high-speed control unit. This unit must be plugged into the mounting box. Transfers of data do not use CPU registers and there is no need for program control except for starting the exchange and testing the status after completion. At the beginning of a transfer the program uses a WER instruction to load the starting address and block length into the control word register. The DMA logic provides all Bus timing signals to control the data transfers directly between the memory and the high-speed control unit. The logic also updates the control word register for each data word and detects when the complete block has been transferred. The data block transfer is terminated with an SST instruction to get the status.

TRANSFER CPU/EXTERNAL REGISTERS

The use of exchanges between the CPU and external registers to set up an input/output processor within a standard system has already been explained. Exchanges may also be carried out with non-standard control units to enable transfers between the CPU and an external register within a control unit for use by specialized input/output systems. Such systems would operate in a similar manner to the programmed channel and may or may not use the interrupt system to control the timing of exchanges.

Up to 256 external registers may be addressed by the system and the facility enables exchanges in either direction.

Four types of control panel may be used for mounting:

- Full Control Panel
- Extended Control Panel
- Mini Panel
- Portable Panel.

FULL CONTROL PANEL

The Full Control Panel is the standard control panel for the P856M. It is 2U (88.90 mm) high.

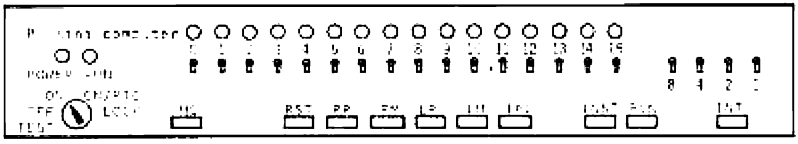


Figure 12.1 Full Control Panel

The facilities available on the full control panel are:

Safety Key Switch
A five position key operated switch providing the main on/off facility. The five positions are:

1. TEST – *Micro diagnostics*
In this position an elementary system test can be performed without any external tool. For a description of the microdiagnostics see page 14-7.

2. OFF – *Power off*

3. ON – *Power on*
In this position an elementary system test can be performed without any external tool. For a description of the microdiagnostics see page 14-7.

4. ON/RTC – *Power on/RTC on*
In this position the CPU is able to run with the Real Time Clock on. All the remaining control panel switches are effective.

5. LOCK – *Power on/RTC on*
In this position the CPU is in run mode with the Real Time Clock on. All the remaining control panel switches with the exception of the INT button are inhibited.

Display Lamps

1. Power Lamp
Situated above the Safety Key Switch, lit when the Safety Key Switch is in all but the Off position and power is being supplied to the system.

2. Run Lamp
Situated above the Safety Key Switch, lit when the CPU is operating in Run mode.

3. Data Lamps
Sixteen lamps situated one above each data switch and numbered 0 - 15. The lamps are lit to indicate the contents of the registers, memory, or status word depending on the settings of other control switches. A 1 bit is indicated where a lamp is lit.

Data Switches
Sixteen numbered data switches. Each switch is a two position switch used for loading the appropriate data bit into a register or memory, depending on the setting of other control switches. A 1 bit is loaded when a switch is in the up position.

Register Address Switches
Four switches mounted to the right of the data switches and used to code the address of the register to be used when reading or loading a register from the Data Switches. The switches are numbered with the address value they represent in binary (8, 4, 2, 1), giving an addressing capability of 0 - 15.

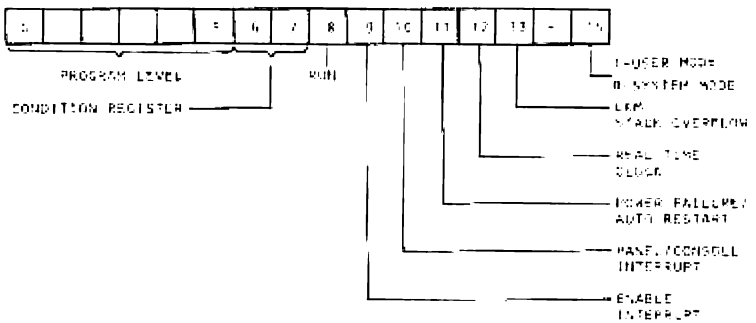


Figure 12.2 Display of status

Control Buttons
The five control buttons are situated nearly centrally beneath the Data Switches. Each button is spring loaded to return to its original position after being depressed and selects and initiates a specific function:

1. RST - *Read Status*
   Depressing this button causes the contents of Program Status Word register (PI.CR.GF.) to be displayed on the lamps.

2. RR - *Read Register*
   Depressing this button causes the contents of the register addressed by the Register Address Switches to be displayed on the Data Lamps.

3. RM - *Read Memory*
   Depressing this button causes the contents of the memory location addressed from the contents of the P Register to be displayed on the Data Lamps. The contents of the P Register are also incremented by 2.

4. LR - *Load Register*
   Depressing this button causes the value set on the sixteen Data Switches to be loaded into the register addressed by the Register Address Switches. The value is also displayed on the Data Lamps.

5. LM - *Load Memory*
   Depressing this button causes the value set on the sixteen Data Switches to be loaded into the memory location addressed from the contents of the P Register. The value is also displayed on the Data Lamps and the contents of the P Register are incremented by 2.

Mode Buttons
The two mode buttons are situated beneath Data Switches 14 and 15. They select and initiate the following modes of operation.

1. INST - *Single Instruction Mode*
   Depressing this button causes the CPU to execute the instruction addressed from the contents of the P Register, and then stop.

2. RUN - *Run Mode*
   Depressing this button causes the CPU to execute the instructions of a program as directed by the program and commencing at the instruction addressed from the contents of the P Register.

Service Buttons
There are three service buttons:

1. MC - *Master Clear*
   Situated beneath Data Switch 0
   Depressing this button raises the master clear level throughout the system whilst it is depressed, causing a general reset of all the associated logic.

2. INT - *Interrupt*
   Situated beneath the Register Address Switches.
   Depressing this button raises a control panel interrupt.
   This button is the only control operative when the Safety Key Switch is in the LOCK position.

3. IPL - *Initial Program Loader*
   Situated beneath Data Switch 10.
   This button will only be present if the IPL option is fitted. In such cases, when the button is depressed it causes the Initial Program Loader to be loaded into central memory and the cpu to be started. Loading is carried out from the device and via the channel specified by the setting of the sixteen Data Switches.

TRANSPORTABLE PANEL

This panel is a free standing full control panel. It is fitted with a connector to enable it to be connected in place of a fixed full control panel or minipanel for mainly servicing purposes.

MINIPANEL

The minipanel may be fitted, on option, to replace the full panel and offers the following facilities:

1. Safety Key Switch
2. Interrupt and Start Buttons
3. Power and Run Indicators.

EXTENDED CONTROL PANEL

The Extended Control Panel is a 4U (177.80 mm) high panel which may be mounted when the CPU is plugged into the 10-slot M4 or M4M box or the 17-slot M5M mounting box (standard for P857M).
This panel permits to have an address and its contents displayed at the same time. Moreover the panel allows debugging facilities as processing may be stopped at any address set previously on the upper row of switches. The user may then load new data.
Addressing from this panel is word oriented.

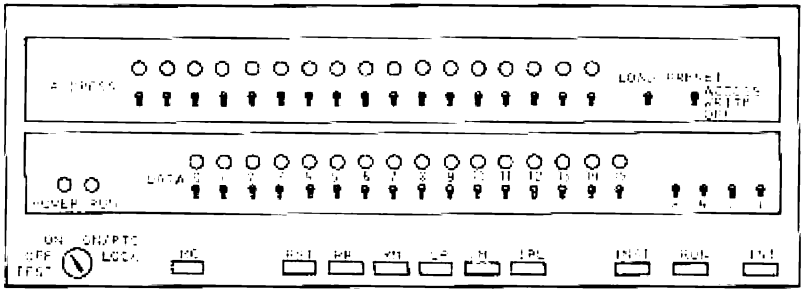


Figure 12.3 Extended Control Panel

The functions of the switches and displays are:

Display lamps
Seventeen lamps situated one above seventeen address switches. When the computer is running the lamps are lit to indicate addresses on the upper part of the panel and data on the display lamps of the lower part. When the CPU stops the contents of the next instruction's address is displayed on the lower part and the address of the instruction on the upper part.

Address switches
Seventeen address switches on the upper part of the panel. Each switch is a two position switch used for loading the appropriate address pattern. A 1 bit is loaded when a switch is in the 'up' position.

LOAD spring-loaded switch
Used to load an address in an address register contained in the control panel. The required address is set on the address switches. The LOAD switch is pressed downwards and the address is displayed on the address lamps.

PRESET switch
A three position switch for debugging purposes:

ACCESS - *stop on memory access*
In this position the CPU stops when a physical address generated by the CPU is identical to the pattern coded on the address keys. If the address is detected the relating instruction is executed and the CPU goes in the idle state.

WRITE - *stop when writing into memory*
In this position the CPU only stops if a store operation is performed in the location whose address was set previously on the address keys.

OFF
The switch is set in this position when debugging is not required.

Reading and loading memory is realised by using the RM and LM buttons. The instruction counter P remains unaffected during these operations as only the address register in the control panel is incremented. It is therefore not necessary to reload P before restarting the program.
The use of the RM and LM buttons is slightly different when the Extended Control Panel is used compared to the description under Full Control Panel.

Read Memory Procedure
- First load the address register with the required address (see LOAD addr).
- Press RM button. The contents of the memory location is displayed on the data lamps.
- The control panel register is incremented by two and the next address is displayed on the address lamps.
  Each time the RM button is pressed the address register is incremented and the contents of the next memory location appears on the data lamps.

Load Memory Procedure
- First load the address register with the address required (see LOAD addr).
- Set the value to be loaded on the data switches.
- Press LM button.
  The value is displayed on the data lamps. The address register is incremented and displayed on the address lamps.

All other pushbuttons and switches have the same meaning as described under FULL CONTROL PANEL.

The basic loading and operating facilities are all carried out at the CPU control panel by the use of the control panel switches. Facilities exist at the panel to enable an operator to load and display selected memory locations and registers, to start the CPU, and to raise a control panel interrupt. In addition an optional facility is available to enable the direct loading of an Initial Program Loader, or similarly written program, from various devices.

PROGRAM LOADING

Program loading may be carried out in 4 separate stages:

1. LOAD BOOTSTRAP - (MACHINE CODE)
2. LOAD INITIAL PROGRAM LOADER - (MACHINE CODE)
3. LOAD SYSTEM OR USER PROGRAM - (OBJECT CODE)
4. LOAD USER PROGRAM - (OBJECT CODE)

Bootstrap
This program is a basic program used to load more sophisticated loader programs. The bootstrap will only load programs which are written in machine code (binary form) and will normally only carry out a checksum to determine errors.

Initial Program Loader
The programs which are classed as initial program loaders are able to load object code clusters into memory and may contain error reporting and other facilities required at the time of loading system or user programs. Initial Program Loaders are written in machine code (binary form) and are loaded using a bootstrap program.

System Programs
Certain of the system programs (monitors) have the facility to load user programs, in these cases the routines within the system program provide the same functions as the initial program loaders.

INITIAL PROGRAM LOADER

The initial program loader provides the system with the ability to automatically load and run an initial program loader, or similar program, from devices connected to the programmed or an input/output processor channel.

Organization
The option consists of a 64-word ROM mounted on the CPU card, and holding a bootstrap program, and the necessary control circuits to load and run the bootstrap using parameters previously set onto the 16 data switches. The parameters set on the data switches are:

bit

0 1 = IPL loaded from ASR, 4 × 4 format
0 = IPL loaded from other devices

1 1 = IPL loaded from disc
0 = IPL loaded from other devices

2 1 . Not used if bit 0 was 0

3 1 = Programmed Channel
0 = I/O Processor

4 - 7 control information for control unit
TY = 0001 MT = 0010
TK = 0111 DK = 0011

8 1 = multiple device control unit
0 = single device control unit

9 1 if disc in system is used

10 - 15device address of device from which IPL is loaded

Where a device has no specific setting requirements on the data switches, for example Cassette Tape, it is sufficient to set the switches to define; 'Other Devices', the correct channel, and the device address and qualification required for the CIO start command.

Operation
The operation of the initial program loader consists of 4 main steps:

1. The bootstrap is copied from the ROM into the first 64 words of central memory.
2. The contents of the 16 data switches are copied into register A15.
3. The CPU is put into INHIBIT INTERRUPT state.
4. The P register is loaded with zero and the CPU started in run mode.

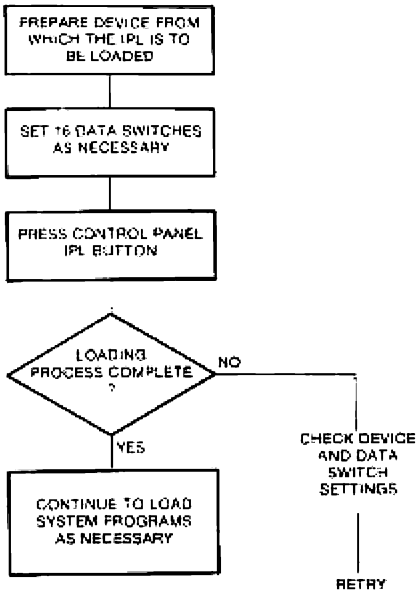


Figure 13.1 Loading the IPL

LOAD MEMORY (FULL CONTROL PANEL)

Figure 13.2 shows the procedure for loading data into memory.

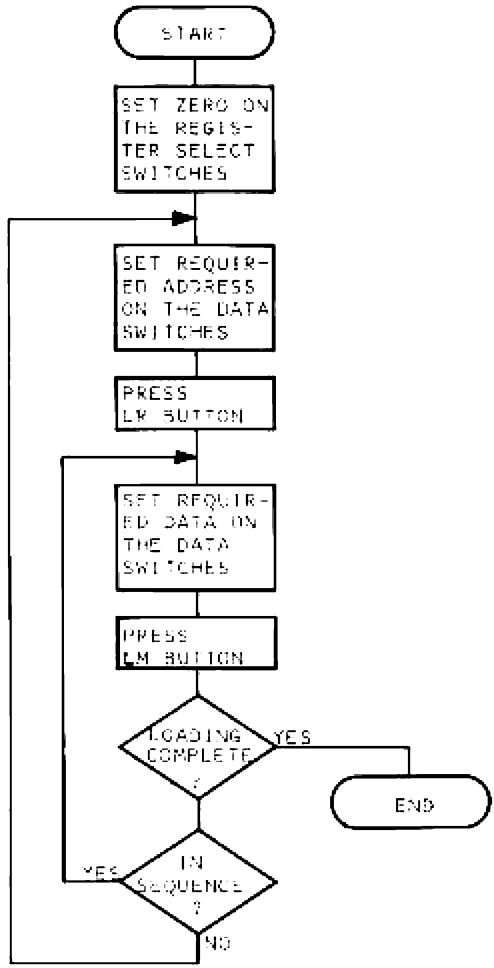


Figure 13.2 Loading Data into Memory

LOAD MEMORY (EXTENDED CONTROL PANEL)

Figure 13.3 shows the procedure for loading data into memory.

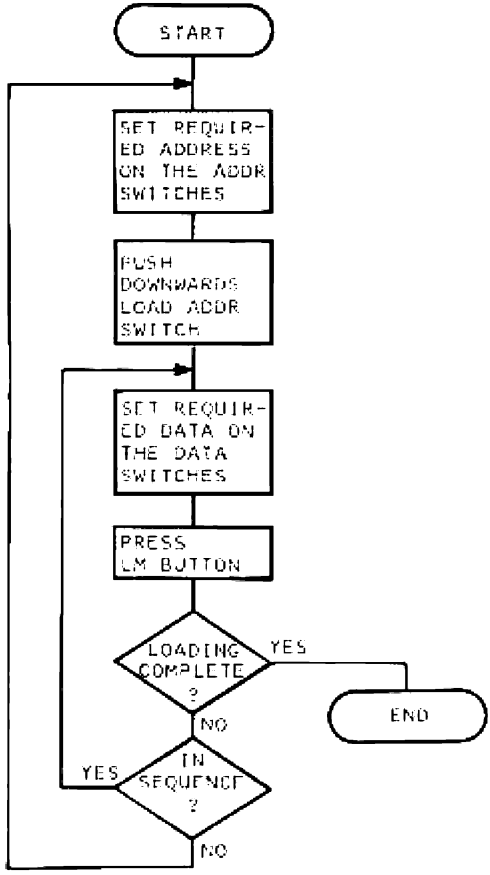


Figure 13.3 Loading Data into Memory

READ MEMORY (FULL CONTROL PANEL)

Figure 13.4 shows the procedure for displaying the contents of memory.

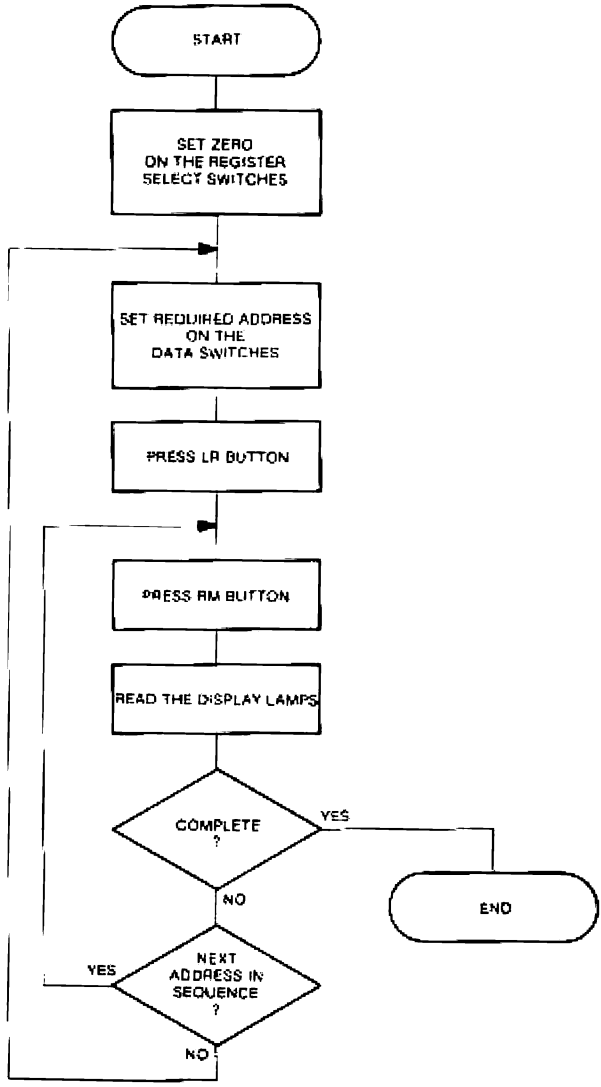


Figure 13.4 Displaying Memory Contents

READ MEMORY (EXTENDED CONTROL PANEL)

Figure 13.5 shows the procedure for displaying the contents of memory.

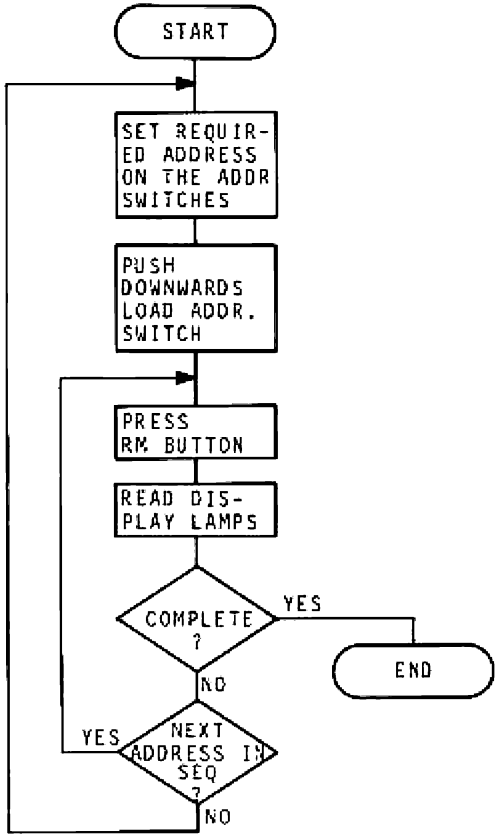


Figure 13.5 Displaying Memory Contents

LOAD REGISTER

Figure 13.6 shows the procedure for loading data into one of the 16 general purpose registers.

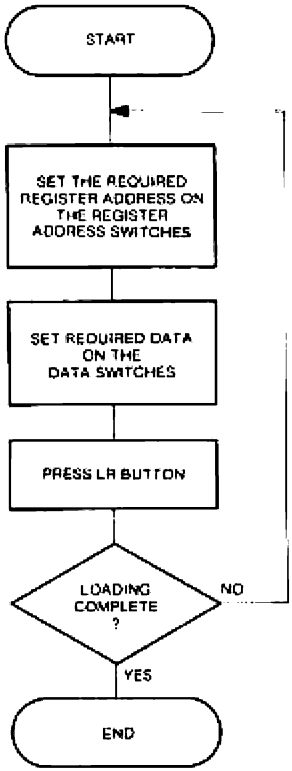


Figure 13.6 Loading Data into Register

READ REGISTER

Figure 13.7 shows the procedure for displaying the contents of one of the 16 general purpose registers. The contents of the program status word may be displayed by pressing the RST button.

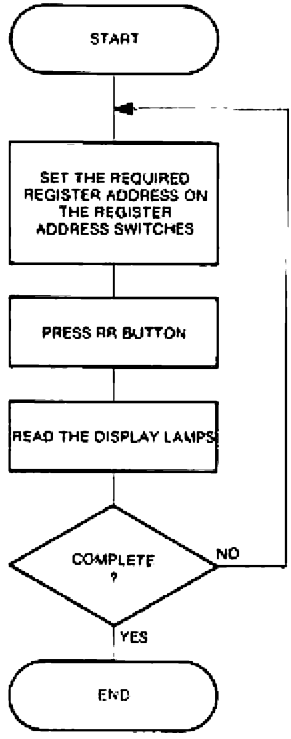


Figure 13.7 Displaying Register Contents

Apart from the main facilities already covered the following additional features are:

1. POWER FAILURE - AUTOMATIC RESTART
2. INTEGRATED V24/V28 SERIAL CONTROL UNIT
3. REAL TIME CLOCK
4. MICRODIAGNOSTICS
5. DETECTION OF PRIVILEGED INSTRUCTIONS

POWER FAILURE - AUTOMATIC RESTART

This facility provides the processor with the ability to terminate processing in an orderly manner after the detection of a power failure, and to restart and resume processing correctly after the restoration of power.

Apart from separate peripherals, all the system's power supplies, whether within the basic cabinet or equipment shelves, are considered necessary for the correct operation of the system. The failure of any of the supplies is therefore able to raise the power failure signal.

Operation

The power failure signal can be connected to any one of the 8 highest priority interrupt levels. When power failure is detected an interrupt is raised and input/output processor exchanges are inhibited, control of the general purpose bus being given to the CPU. Interrupt action takes place and the associated interrupt routine is executed to save the contents of registers, and if necessary specific areas of MOS memory. Core memory is already protected and thus no loss of data from core occurs even if total power failure occurs before completion of the saving routine. On restoration of power the system restarts and CPU operation continues with the restoration of all registers and areas saved before completing the interrupt routine and returning to the originally interrupted program. The power failure interrupt is reset as necessary by the use of the Reset Internal Interrupt (RIT) instruction.

The power failure signal may also be raised at initial power on time if the control panel key switch is set to the LOCK position. In this position the CPU is started and provided the power failure signal is connected to an interrupt level the restoring routine of the level is carried out to restart normal operation at the point it was last suspended.

When the power failure signal is not connected, the CPU will start and remain in the idle state at power on, or after restoration of power following a failure.

Limits
Power failure is set at least 2 ms before the voltage drops below the acceptable limit.

The saving routine should not last more than 2 ms.

Power failure is not set for detected losses of less than 5 ms. The contents of a memory location involved in a memory cycle at the time of total failure is not guaranteed.

REAL TIME CLOCK

A real time clock is available within the system, control of the clock being provided by the control panel key:

ON - RTC stopped
ON RTC - } RTC running
LOCK - }

Once running the RTC generates a signal with reference to the main power supply frequency and is not able to be stopped by program. The generated signal may be connected to any of the 8 highest priority interrupt levels and is thus able to raise an interrupt every 20 ms for 50 cps supplies or 16.67 ms for 60 cps supplies. The associated interrupt must be cleared using the Reset Internal Interrupt (RIT) instruction and the RTC routine may be used as required within the system.
An optional programmable real time clock is available on one board, requiring one slot in the mounting box.

INTEGRATED V24/V28 SERIAL CONTROL UNIT

A V24/V28 Serial Control Unit is available within the system mounted on the CPU board. This control unit allows to attach one of the following asynchronous peripherals as I/O console:

- ASR
- PER3100 } with V24 interface
- Display

The transmission speeds are 110, 600, 1200, 2400, 4800 or 9600 bps.
The speed selection is made by straps on the card. Also selected by straps may be the parity; odd, even or no parity. Odd or even parity is generated or checked by the controller. The number of stop bits, one or two, is also selectable by straps and are generated by the controller.

Organisation

Operation of the control unit is only possible via the programmed channel through the general purpose bus. Connection from the control unit to the peripheral must be according the V24/V28 recommendations.

Data are transferred serially to the control unit and is carried out in parallel by the use of OTR/INR instructions, bits 8 - 15 of a specified register being used.

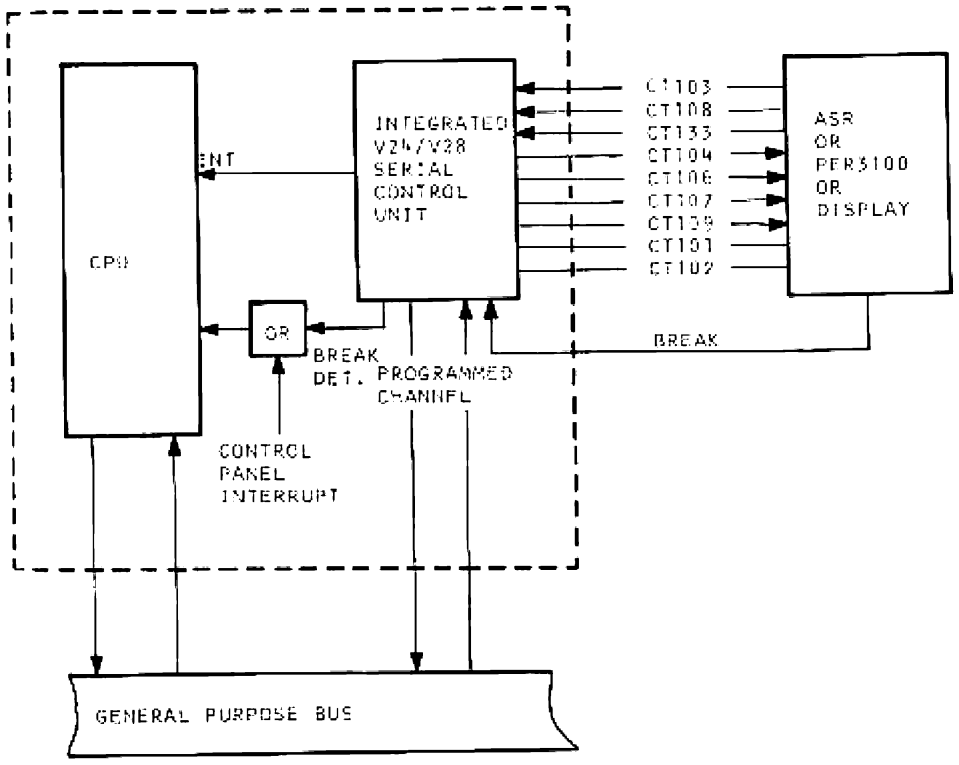


Figure 14.1 Integrated serial control unit

Break feature
Pressing the 'Break' key on the peripheral's keyboard is always accepted by the serial control unit. The activated interrupt is 'ORed' with the Control Panel interrupt.

Operation
The control unit operates in the same manner as other control units, commencing in the inactive state, transferring during the exchange and execute states, and stopping in the wait state. Operation may be in either wait or interrupt mode. Input/output instructions recognizable as commands to the unit are:

CIO	START	input/output
CIO	STOP	
OTR		
INR		
SST		

Responses to these commands are set into the condition register in the normal manner.

The interrupt generated when the control unit is in the exchange or wait states may be connected to any one of the 8 highest interrupt levels and such an interrupt is cleared by the sending of an appropiate I/O command to the unit.

Figures 14.2 and 14.3 show flowcharts of possible methods of programing the V24 controller.

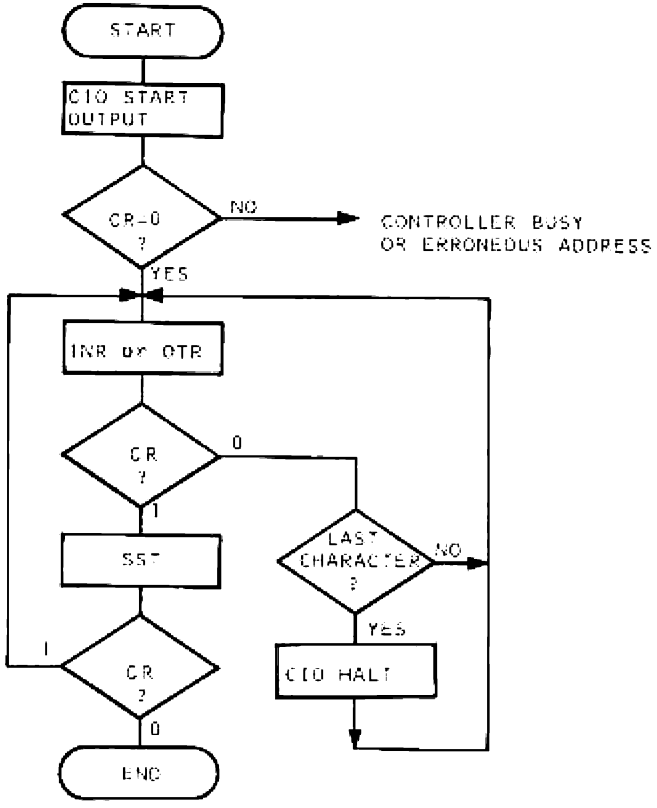


Figure 14.2 Wait mode

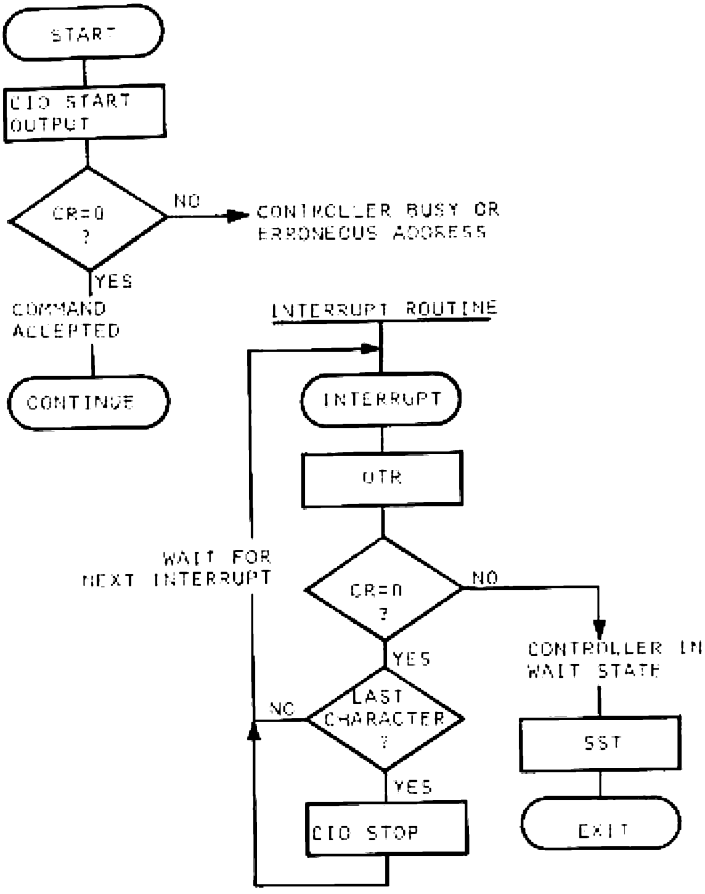


Figure 14.3 Interrupt mode

MICRODIAGNOSTICS

The P856M and the P857M contain an automatic testing feature in the form of a microprogrammed diagnostic built into the CPU logic. Successful running of the tests indicate that sufficient parts of the CPU function for loading of test programs.
The microdiagnostics for the P856M test the first 4k of memory and for the P857M the first 16k of memory. The prerequisite tool is the FULL CONTROL PANEL or the EXTENDED CONTROL PANEL, as the results of the tests are displayed on the data lamps.
About 100 words are reserved for the microdiagnostic program.
The test can only be performed when the key in the key switch is in the TEST position.

Test Procedures
Before starting any test, except for steps A to D included in the Test 2, the user has to set a control unit address on data switches 2 to 7 included to check the dialogue through the Bus between the CPU and the control unit.

Test 1 Automatic Test
This is a fast check which automatically goes through a number of operations. If the tests have been satisfactory special codes are displayed on the data lamps.

- set data switch 0 to 0
- set a control unit address on data switches 2 thru 7
- press RUN button
- wait for display of code no 4
  code 4: data lamp 12 off
  all other lamps lit
  if this code is not displayed go to Test 2
- press LM button and wait for display of code 5
  code 5: all lamps lit
  If the code is not displayed go to Test 2.

Test 2 Step-by-step testing
This sequence may be used if Test 1 showed an erroneous display or if the user wishes to perform separate tests. In these tests the user verifies the operation of the control panel up to the memory.

A. Control Panel test
Each data key and the lamp above it are tested by setting the key in the 'up' position after which the lamp must be lit.
Press LR button to go to the next step.

B. L register test
This step includes the GP BUS and the L register in the test. The operator

may use the switches in the same way as described under control panel. Press LR button to go to the M register test.

C. M register test
This step includes the M register (through the C selector and ALU) in the thest. The operator may use the switches in the same way as described under control panel. Press the LR button to go to the Q register test.

D. Q register test
This step includes the Q register in the test. The operator may use the switches in the same way as described under control panel.

From this moment on the operator may choose among three data path tests, an instruction simulation test or a memory test by setting on the data switches a hexadecimal number and a control unit address, followed by pressing the LR button.
If the relevant test is executed without errors the data lamps display a certain code.

It is possible to skip the visual tests A thru D. The user must then set switch 0 to 0, set a control unit address on switches 2 thru 7, and set switch 15 to 1. Next press the LR button 4 times. Then wait for display of code 1. Press LR button and wait for display of code 2. Press LR button and wait for display of code 3. Press LR (or RUN) button for display of code 4. Press LM (or LR) button for display of code 5.

Test 3 Chained test
In this mode the hardware is tested in a loop which may be stopped by operation of data switch 0.

- set data switch 0 to 1, a control unit address on switches 2 thru 7, and switch 15 to 1.
- press LR button 4 times. The microprogram starts looping.

To stop the loop:
- set switch 0 to 0.
  One of the 5 codes as listed above is displayed. If it is not code 5 press the LR button as many times until code 5 appears.

To restart the loop set switch 0 to 1.
To restart at the beginning of the test turn the key in the key switch to OFF and next to TEST. Set switch 0 to 1, set the control unit address, and set switch 15 to 1 and continue as described above.

	Hexa no on data switches	Test functions	Display on data lamps when no fault is found
data path test	/0001 + CU address	- shift left Q reg. - bus A selection - constant 'TWO' - QO test - A or B, A+B and B inverted ALU functions - ALU = 0	code 1 lamp 15 OFF all other lamps lit
data path test	/0002 + CU address	- shift right Q reg. - ALUZERO - A-B, A+B and crossed A ALU functions - constant 'TEN' - P reg, P = 2 function	code 2 lamp 14 OFF all other lamps lit
data path test	/0004 + CU address	- A operand shifted right - 4 x A function - reading and writing scratch pad	code 3 lamp 13 OFF all other lamps lit
instruction simulation	/0008 + CU address	DLA - K is loaded with DLA code - values loaded in A1 and A2 - branch to DLA micro program - return to microdiagnostic program RB K is loaded - RB microprogram next address generated by PLA	code 4 lamp 12 OFF all other lamps lit
memory test	/0010 + CU address	- bit 15 is set to 1 in all addresses of a 4k/16k block - the block is read and verified - the 1 is shifted left 1 position etc. next: - all words of a 4k/16k block receive their address values as contents these values are verified - tests the TMP-TPM dialogue	code 5 all lamps lit

DETECTION OF PRIVILEGED INSTRUCTIONS

The central processor may operate in two modes:
- system mode
- user mode

System Mode
All available instructions may be executed and the whole memory is accessible. The programmer may use privileged instructions which modify the CPU state namely, the I/O instructions, External transfer instructions and instructions modifying the contents of the stack pointer A15.
The monitor and system programs are executed in this mode.

User mode
User programs operating under monitor control are executed in this mode and any attempt to execute a privileged instruction causes the Trap action to be activated (see page 7-5).
If, however, system allocation is required an LKM instruction sets the CPU, through the monitor, in the system mode.
When the CPU is operating in user mode bit 15 of the PSW is set to 1.

Data Communication

A full range of data communication control units for synchronous and asynchronous transmission makes use of the latest LSI technology for increased performance and reliability.

All control units may be plugged in the mounting box or equipment shelf to allow systems to be built easily. A diagnostic box permits the user to verify his system.

The following data communication control units are available:

SLCU2S P847-060	A synchronous double-buffered line control unit which controls one full duplex line or two half duplex lines. It handles 5, 6, 7 or 8 bit characters at a maximum speed of 200,000 bits per second on inplant lines or 20,000 bits per second for outplant lines. The modem interface is V24/V28.
SLCU4 P847-070	A synchronous double-buffered control unit which handles two full duplex lines or four half duplex lines. It recognises 5, 6, 7 or 8 bit characters at a maximum speed of 100,000 bps for inplant lines or 9,600 bps for outplant lines. The modem interface is V24/V28.
AMA8A P845-060	An asynchronous multiplexor for 8 half duplex or 8 full duplex lines. The following speeds are possible: 50, 75, 100, 110, 150, 200, 300, 600, 1200, 2400, 4800 or 9600 bps selectable per line. The control unit recognises 5, 6, 7 or 8 bit characters. The modem interface is V24/V28.
AMA8C P845-070	This control unit is similar to the AMA8A but designed for inplant use. Each line has a four wire current loop interface or a TTL compatible interface.
ALCU2 P846-060	Asynchronous line control unit for handling one full duplex line or two half duplex lines. It recognises 5, 6, 7 or 8 bit characters. The line speed is selectable 300, 600, 1200, 2400, 4800 or 9600 bps.
ALCU4 P846-070	Asynchronous line control unit for handling two full duplex or four half duplex lines. The other features are the same as for the ALCU2.

The following modules are available:

D-MODULES

Input:	Digital Input Solid-state Module
	Digital Input Priority Interrupt Module
	Digital Input Isolating Module
	Digital Input Counter Module
	Time Interval and period Module
Output:	Digital Output Solid-state Module
	Pulse Output Control Module
	Analog Output Fast Module
	Analog Output Control Module

A-MODULES

Analog Scan Control Module
Analog Input Solid-state Module
Analog Input low-level Module
Analog Input high-level Module

P857M in M4M mounting box

CABINETS

The basic cabinets contain standard 19" racks which are used to hold mounting boxes, equipment shelves and various peripheral equipment. The mounting boxes and equipment shelves are able to contain and provide system d.c. power and cooling to the printed circuit boards fitted within them. Each mounting box has dedicated locations for the fitting of the processor cards and the first memory module. Figure 16.2 shows the possible layout of equipment within the cabinet and includes:

Central Processing Unit
Paper Tape Reader
Paper Tape Punch
Cassette Tape Units
Moving Head Disc Units.

BASIC MOUNTING BOX AND EQUIPMENT SHELVES

M1 Mounting Box (for up to 16k P856M)

Number of slots	4 sub-assembly slots for cards connected directly to the GP Bus.
Size	Height 3U (approx. 132.5 mm), depth 585 mm.
Power Supply	+5 V 15A –5V 0.8A +16V 4.5A ±18V unregulated, 1A

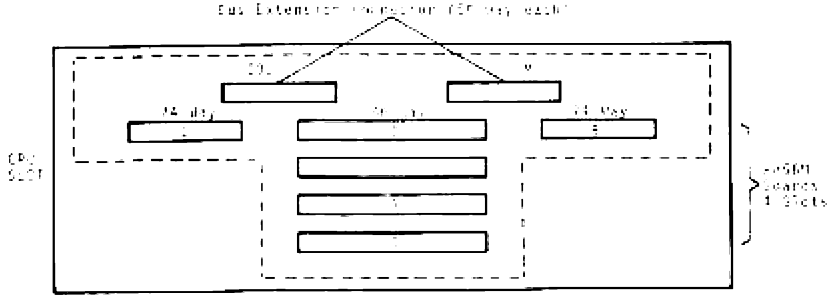


Figure 16.1 M1 Mounting Box Backplane Arrangement

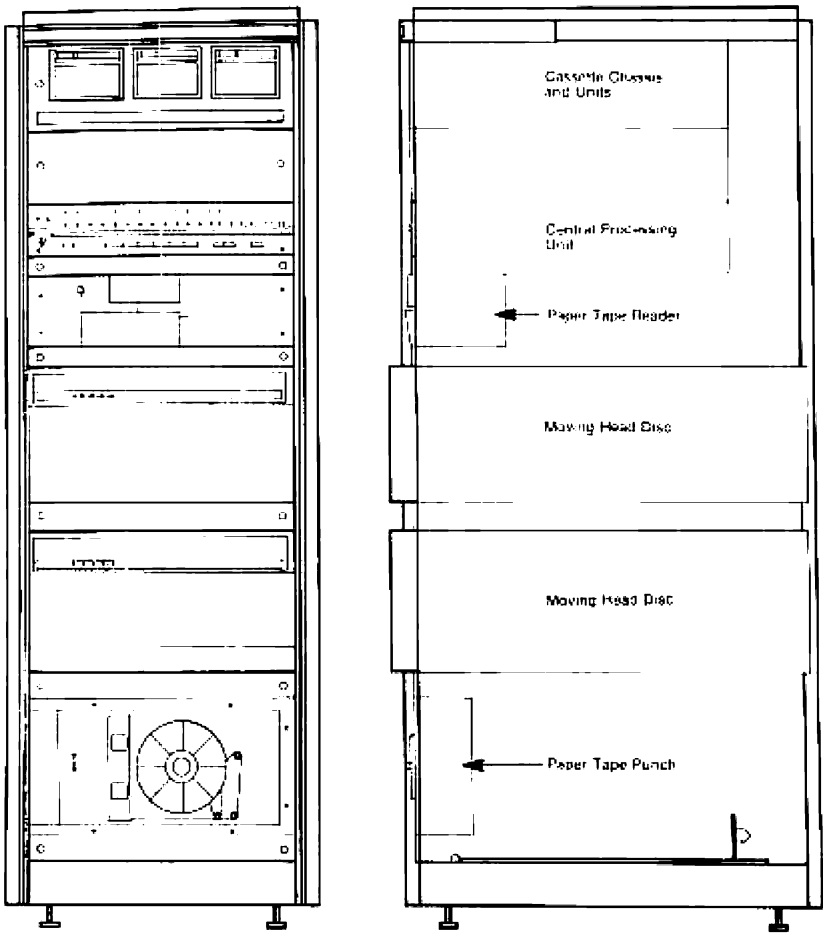


Figure 16.2 Example of Equipment Mounted in a Cabinet

M4 Mounting Box (for up to 32k P856M)

Number of Slots : 10 sub-assembly slots for cards directly connected to the GP Bus.

Size : Height 6 U (approx. 265 mm), depth 550 mm.

Power Supply : +5V, 43A
−5V, 1.6A
+16V, 8.5A
±18V, unregulated, 2A

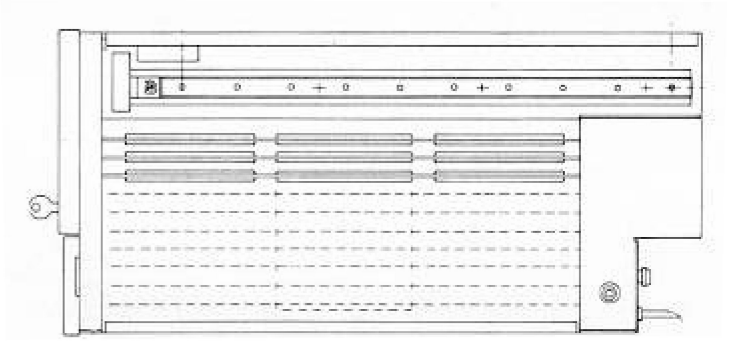


Figure 16.3 M4 Mounting Box Side View

M4M Mounting Box (for up to 64k P857M)
This is the same mounting box as the M4 mounting box but contains extra wiring for the MMU board.The CPU must be plugged in the first slot, the MMU in the second and the FPP in the third slot.

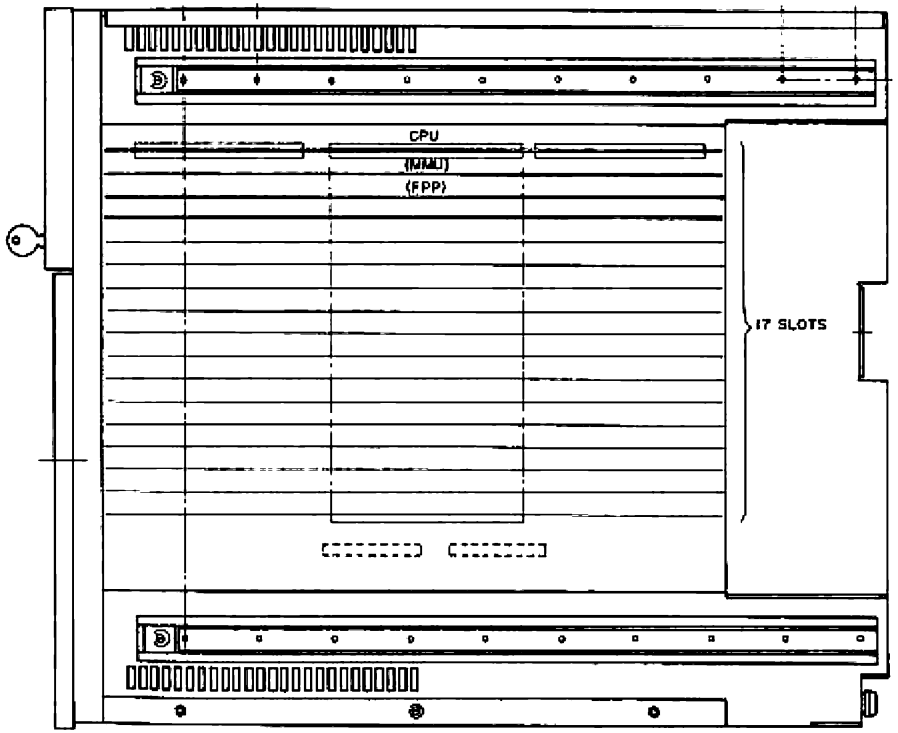
M5M Mounting Box (for up to 128k P857M)

Number of Slots : 17 sub-assembly slots for cards directly connected to the GP Bus.

Size : Height 11 U (approx. 489 mm), depth 550 mm.

Power supply : +5V, 86A
−5V, 4A
+16V, 17A
±18V, unregulated, 4 A.

For power consumption reasons it is advised not to plug more than 4 memory modules in 4 of the first 10 slots. Other memory modules may be plugged into slots 11 thru 17.



Equipment Shelf P843-001

Number of Slots : 6 sub-assembly slots for control units connected directly to the GP Bus.

Size : Height 3U (approx. 132.5 mm).

Power Supply : +5V 18A
+18 V 2A
-18V 2A

Other Facilities Where the Equipment Shelf is situated at the end of the GP Bus a termination is necessary. The Bus can be terminated by the inclusion within the shelf, of the required termination boards.

Interconnection between units

The interconnection between units is carried out via the backplane wiring within the mounting box and the equipment shelves and by the use of signal cables between the control units and devices. Interconnection between the mounting box and equipment shelf is carried out by the GP Bus and Break Line cables. GP Bus and Break Line cable connectors being fitted on the backplane of the mounting box and equipment shelf. Where necessary it is also possible to extend the GP Bus and Break Line cables to self contained control units.

INSTALLATION

All the standard units of the system have been designed for straight forward installation, and in most cases very few or no special considerations will be necessary, either with reference to the layout of the equipment, or to the installation site itself. However, because of the flexibility, and therefore widely differing possibilities for system configuration, each site must be planned and installed with reference to its own configuration. The detailed information required for any installation may be found in the Installation Manual and associated publications dealing with the peripheral devices to be used.

Electrical Supplies

Systems are supplied for connection to a mains supply which should be wired for the use of the system only. The supply requirements are:

System 3 wire: single phase, neutral and earth, or two phases and earth.

Voltage 100V, 115V, 220V or 240V ± 10%. Standard is 220V.

Frequency 50 ± 2 Hz or 60 ± 3 Hz.

Power — The supply circuit should be designed to adequately meet the current requirements of the system, and where expansion is envisaged sufficient capacity to meet the expansion should be provided at the time of initial installation to avoid major power re-organization.

Environmental Control
The requirement for environmental control will depend entirely on the configuration and siting of the system and may vary from a normal office environment for the smaller non-magnetic orientated systems to full air conditioning for sophisticated magnetic systems.

The general operating conditions normally accepted within the computer room are listed below but in all cases the requirements of any of the equipment within the system, which is not within these tolerances, must be met.

Temperature	- 0°C to +45°C.
Relative Humidity	- up to 90% without condensation.

Safety
The individual units which comprise a standard system have been designed to meet necessary safety standards. Safety precautions for non-standard units and the system as an installation will depend on local regulations and conditions, and should be designed to adequately cover the initial installation and any future planned expansion.

INTERFACING

As all interfacing between the units of the system is carried out via the general purpose bus, the design of peripheral control units, whether for standard or non-standard devices, is made easier. Interfacing circuits within control units are designed to the same specification, and as timing is carried out within the bus circuitry on a signal and response basis, then timing control circuits within control units may be reduced. Control units for connection directly to the GP Bus and for controlling basic peripherals are available, in certain configurations, combined on one multiple control unit board, whilst control units for the more sophisticated magnetic peripherals are available on separate boards.
Complete details of all interfacing requirements may be found in the Interface Manual, which should be used whenever exact references are required.

A comprehensive range of standard peripheral equipment is available for use within the system, and where it is required non-standard and customer built devices may be connected either separately or in conjunction with standard equipment.
The standard peripheral devices currently available includes:

Input/Output Typewriters
P841-101 Normal ASR typewriter including paper tape reader/punch, current loop interface.
P841-105 The same as P841-001 but with V24 interface.
P842-001 PER3100 Matrix printer with keyboard, V24 interface.
P842-002 PER3100 Matrix printer with keyboard, current loop interface.

Punched Tape Equipment
P801-001 Punched Tape Reader, 333 char per sec.
P802-001 Punched Tape Reader, 600 char per sec.
P803-001 Tape Punch, 75 char per sec.

Card Reader
P806-102 Punched card reader, 300 cards per minute.

Line Printers
P809-002 Matrix line printer, 200 lines per minute, 132 col.
P811-001 Line printer, 245 lines per minute, 132 col.
P812-001 Line printer, 670 lines per minute, 132 col.
P842-003 PER3100 Matrix printer without keyboard, V24 interface.
P842-004 PER3100 Matrix printer without keyboard, current loop interface.

Cassette Tape Equipment
P833-001 Cassette tape drive unit, 7.5 ips, 800 bpi.

Magnetic Tape Equipment
P831-002 Magnetic tape drive, 25 ips, 800 bpi, 9-track.
P831-004 Magnetic tape drive, 45 ips, 800 bpi, 9-track.
P831-006 Magnetic tape drive, 37.5 ips, 1600 bpi, 9-track.

Magnetic disc equipment
P824-002 Moving head disc drive, 2.7M bytes
P825-007 Moving head disc drive, 40M bytes

Display Equipment
P818-001 Display, current loop interface.
P818-002 Display, V24 interface.

POWER SUPPLIES

The necessary power supplies for all the standard peripheral devices are produced by either self-contained power supply units or by a separate unit mounted together with the device in either the basic cabinet or an equipment shelf. Power supplies for the associated control unit are derived from the power supplies within the mounting boxes and equipment shelves or from the peripheral's separate power supply.

CONNECTION TO THE SYSTEM

The connection of standard peripheral devices to the system is carried out using a control unit and transfers will take place via the programmed or an input/output processor channel. Using either the programmed or an input/output processor channel, transfer rates up to the maximum operating speed of the device are possible and in normal circumstances these rates will always be maintained, the rate only being reduced when the servicing of the programmed or input/output processor channel concerned is slow.

CONTROL UNITS

Certain control units which are connected directly to the general purpose bus are of a multiple type (MCU), that is more than one control unit is mounted on a single printed circuit board. The configuration of MCU's and the availability of control units for connection to the system are:

Multiple Control Units (MCU's)
Multiple control units for use with PTR, PTP, V24 serial CU, LP and CR are available in the following configurations:
1. PTR/PTP/V24 serial CU.
2. PTR/PTP.
3. LP/CR.

CU's for all the devices mentioned above except the PTP and CR are also available as single control units.

Connection details for standard control units

Type Number	CU	Channel Connection		Int/ Breaks	Remarks
		Prog. Chan.	I/O Proc.		
P801-040	PTR	x	o	1	separate CU
P840-001	PTR PTP	x x	o o	2	multiple CU
P840-002	PTR PTP V24	x x x	o o o	3	multiple CU
P840-003	CR LP	o o	x x	2	multiple CU
P810-040	LP	o	x	1	separate CU
P845-040	V24	x	o	1	separate CU
	V24	x	-	1	integrated on CPU
P831-040	MT	o	x	1	CU for 4 drives
P824-040	Disc	-	x	1	CU for 2 drives
P825-040	Disc 40 Mb	-	x	1	CU for 2 drives
P833-152	Cass Tape	x	x	1	CU for 3 drives
P837-001	DIOD 2 words	o	o	1	
P837-002	DIOD 4 words	o	o	2	
P847-060	SLCU2S	x	x	2	
P847-070	SLCU4	x	x	4	
P846-060	ALCU2	x	x	2	
P846-070	ALCU4	x	x	4	
P845-060	AMA8A	x	x	2	
P845-070	AMA8C	x	x	2	
P844-060	AMA16	x	-	1	
P844-110	V28CM	x	-	1	

Note: o means that connection to the channel is possible but not supported by standard software.
x connection supported by standard software.
- connection not possible to the channel.

The connection of non-standard devices to the system must also be made via a control unit and standard boards are available on which the customer may assemble his own control units. Boards are available without any logic circuits (printed circuit boarding) or with standard address and function decode logic and interrupt encoding already mounted and connected (General Purpose Cards).

INPUT/OUTPUT TYPEWRITERS

P841-101 Typewriter

Figure 17.1 shows the P841 typewriter.

Figure 17.1

The P841-101 is a normal duty typewriter (ASR33) with attached paper tape reader/punch equipment. All the facilities operate at a maximum transfer speed of 10 characters per second, and may be operated on or off line to the system, switching being carried out at the typewriter.

Connection to the System

Connection to the system is with current loop interface.

Main Controls

Mode Switch – A three position switch mounted on the front of the typewriter, used to control the mode of operation of the typewriter.

OFF	Typewriter switched Off.
LOCAL	Typewriter and paper tape equipment are operative but are not connected to the system.
LINE	Typewriter and paper tape equipment are operative and connected to the system.

Paper Tape Reader Switch – A three position switch mounted on the top of the paper tape reader.

START	Paper tape reader is started manually if the Mode Switch is in either the LINE or LOCAL position.
NEUTRAL	Paper tape reader is operative and may be started or stopped.
STOP	by the system if the Mode Switch is in the LINE position. Paper tape reader is stopped manually by pressing the switch towards the free position.
FREE	The paper feed is freed and the tape may be repositioned in the reader without completely releasing it from the mechanism.

Paper Tape Punch Controls – Four individual push button controls mounted on the top of the punch.

ON	The punch is started manually if the Mode switch is in either the LINE or LOCAL position.
OFF	The punch is stopped manually.
	Note. The punch may be started and stopped by the system if the mode switch is in the LINE position.
REL	The tape is released and may be threaded through the punch as required.
BS	The tape is back spaced one character each time the button is depressed. This facility should only be used when the punch is operating LOCAl and is stopped.

Basic Specifications

Operating Speed	- 10 characters per second.
Size	- Width 560 mm, Height 1140 mm, Depth 470 mm.
Weight	- 25 Kilograms.
Paper Width	- 216 mm.
Power	- 300 VA.

Operating Temperature - 0 - 45°C.
Relative Humidity - 20 - 80%.

P841-105 Typewriter
This typewriter is the same as the P841-101 but with V24 interface. It may be connected to the integrated V24 control unit or the multiple control unit, or asynchronous Data Communication control units.

P842-001 PER3100 Matrix Printer
Figure 17.2 shows the P842-001 matrix printer and keyboard with V24 interface.

The P842-001 matrix printer and keyboard offers the same basis facilities as the typewriter without attached paper tape equipment. It is capable of near silent operation at up to 50 characters per second and may use peg or friction fed paper of various widths, multiple copies being available when peg fed paper is used.

Figure 17.2

Line spacing of 1, 1½, or 2 normal lines and LOCAL/ON LINE/OFF operation are selectable at the printer. Various keyboard layouts and character sets are available, including the possibility of up to 7 special characters on option.

Connection to the System
Connection to the system may be via the programmed or input/output processor channel and is made via the V24 serial control unit.
In all cases the maximum printer speed is 50 characters per second although the actual speed of transfer will depend on the control unit, interfacing, and program being used. The available interface boards enable: transfer speeds of 100-9600 baud to be selected in specific steps. Where transfer rates of above 50 characters per second occur or in the case of certain special characters the controlling program must insert sufficient null characters to avoid the loss of data.

Main Controls
Power On/Off Switch – An external two position switch, used by the operator to switch the mains power to the printer On or Off.

Operational Switch – An external two position switch, used by the operator in certain cases to make the printer operable.

Continuous Line Feed Switch – An external spring loaded switch, which whilst depressed causes line feeding of the paper to occur continuously.

Apart from the mentioned switches internal links exist on the standard interface boards within the printer, for the selection of line speed and to enable an echo print facility if this is required.

Basic Specifications

Operating Speed	– Up to 50 characters per second.
Size	– Width 510 mm, height 170 mm, Depth 310 mm, without keyboard, 465 with keyboard.
Weight	– 20 Kilograms.
Paper Width	
Peg Fed	– 231.8 mm, 203.2 mm and 314.3 mm (perforation distance).
Friction Fed	– 148 mm to 306.3 mm.
Power	– 100 VA Average.
Operating Temperature	– 10° - 40°C operating.
Relative Humidity	– 20 - 80% operating.

P842-002
This is the same printer as the P842-001 but with current loop interface and the following additional switches:
Line Spacing Switch - A three position switch mounted on the KSR interface board and used to select the required line spacing when the KSR interface board is fitted.

Mode Switch - A three position switch mounted on the KSR interface board within the printer and easily accessible by the operator. The switch is used to control the mode of operation of the printer when the KSR interface board is used:

OFF	Printer does not accept either line or keyboard inputs. The main power supply to the printer is not effected by this switch and may be ON.
LOCAL	Printer interface is operable from the keyboard only, no line signals are sent or accepted by the printer.
ON LINE	Printer interface is operable and may accept both line and keyboard inputs. Keyboard inputs are also retransmitted as line outputs.

P842-003 As P842-001, but without keyboard.
P842-004 As P842-002, but without keyboard.

PUNCHED TAPE EQUIPMENT

P801-001 Punched Tape Reader

Figure 17.3 shows the P801-001 Punched tape reader.

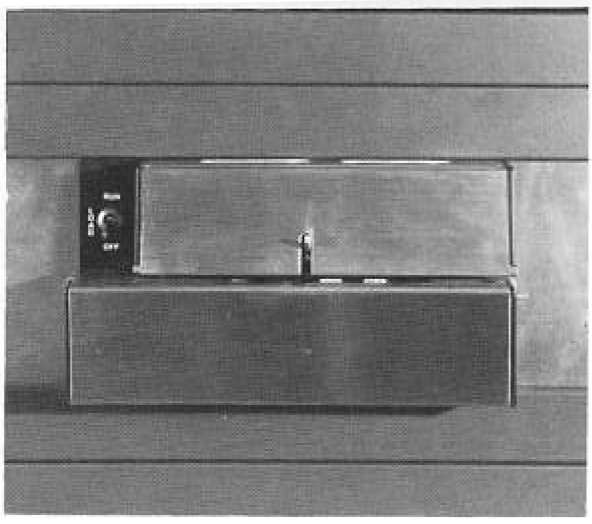


Figure 17.3

The P801-001 punched tape reader provides the system with the ability to read a wide range of punched paper tapes at a speed of up to 333 characters per second.

The reading assembly is of the photo-electric type and raises data and timing signals at TTL levels, 8 data channels and 1 timing channel being available. The Tape drive unit controls the movement of the tape across the readhead via a drive motor and associated pinch roller and brake assemblies. No adjustment to the pinch roller is necessary when tapes between 0.064 to 0.124 mm (0.0025" to 0.005") thick are used and adjustment for 17.5 mm, 21.4 mm, or 25.4 mm (11/16", 7/8", or 1") wide tape is carried out by an externally mounted control.

Connection to the System
Connection to the system may be via the programmed or an input/output processor channel.

Mounting
The complete reader, including power supply, is assembled for mounting in a standard 19" rack and may be fitted into either the basic or an extension cabinet.

Main Controls
Power Switch – A three position switch mounted on the front panel of the reader, used for switching the power on the reader:

OFF	No power is switched on to the reader.
LOAD	Power is supplied to the drive unit motor and reading unit, the pinch roller and brake assemblies are clear of the tape track to allow loading.
RUN	Power is supplied to all the reader circuits and the reader operates under the control of the system.

Tape Width Selector – An adjustable control mounted on the side of the reader. The control is lockable and is used to adjust the tape guide mechanism as required.

Tape Load Lever – An external control on the front of the reader, used to disengage the front tape guide and allow insertion of the tape.

Basic Specifications

Operating Speed	– 333 characters per second.
Size	– Width 483 mm, Height 133 mm, Depth 203 mm.
Weight	– 15 Kilograms.
Tape Size	– Width 17.5 mm, 21.4 mm, 25.4 mm (11/16", 7/8", 1") selectable.
	– Depth 0.064 to 0.124 mm (0.0025" to 0.005") 14.12
Power	– 150 VA.
Operating Temperature	– 0 - 45°C.
Relative Humidity	– 20 - 80%.

P802-001 Punched Tape Reader
In all respects apart from maximum operating speed the P802-001 is the same as the P801-001 Punched tape reader.

Operating Speed	– 600 characters per second.

P803-001 Paper Tape Punch
Figure 17.4 shows the P803-001 Paper Tape Punch.

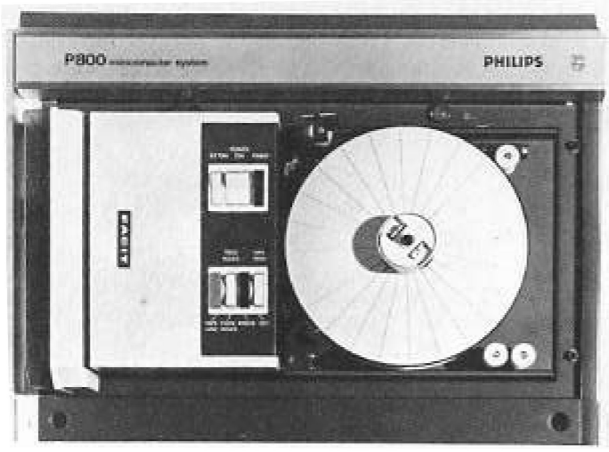


Figure 17.4

The P803-001 paper tape punch provides the system with the ability to produce a punched paper tape output at a rate of up to 75 characters per second on various width tapes. No adjustment is necessary for tapes of 0.08 to 0.11 mm (0.0031" to 0.0047") thickness and the punch may be set to accept tape of between 17.5 mm 11/16") and 25.4 mm (1") in width. Both supply and take up bobbins are fitted and can be used with reels of tape up to 20 cm in diameter. The punch includes its own power supply.

Connection to the System
Connection to the system may be via the programmed or an input//output processor channel.

Mounting
The punch is available assembled for mounting in a standard 19" rack or as a free standing unit.

Main Controls and Indicators

Power On Switch – A two position switch mounted externally, used to switch the mains power to the punch On or Off.

DC On Switch – A two position switch mounted to one side of the Power On switch, used to switch the internal d.c. supply to the punch.

Tape Feed Switch – A two position switch mounted externally and spring loaded to the off position. When the switch is depressed tape is fed from the supply reel to the take up bobbin without punching.

Feed Holes/Code Switch – A three position switch mounted externally and spring loaded to the central, off, position. When the switch is depressed tape is fed from the supply reel to the take up bobbin and either feed holes only or feed holes and code holes in all tracks are punched, with respect to the depressed position of the switch.

Apart from the main controls, indicator lights are mounted externally to indicate: d.c. power on, supply tape low, and certain errors. Internal switches are also fitted to control the take up bobbin.

Basic Specifications

Operating Speed	– 75 characters per second
Size	– Width 330 mm, height 190 mm, Depth 432 mm.
Weight	– 13 Kilograms.
Tape Size	– Width 17.5 to 25.4 mm (11/16 to 1") Thickness 0.08 to 0.1 mm (0.0031" to 0.0043").
Power	– 180 VA max.
Operating Temperature	– 0 - 45°C operating.
Relative Humidity	– 20 - 80% operating.

CARD READER

P806-102 Card Reader

Figure 17.5 shows the P806-102 card reader.

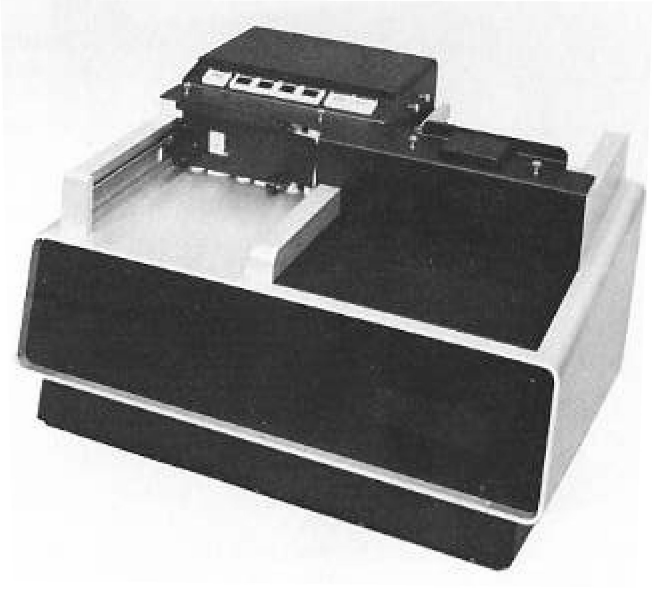


Figure 17.5

The P806-102 card reader provides the system with the ability to read data from 80 column cards at a transfer rate of up to 300 cards per minute. Card handling facilities in the form of an input hopper and output stacker enable the reader to handle up to 1000 cards without operator intervention for loading. The reader is of the photo electric type and employs a straight through card track with a vacuum picking mechanism, providing almost jam free operation and extremely long card life.

The reader is free standing and includes its own power supply.

Connection to the System
Connection to the system may be via the programmed or an input/output channel.

Main Controls
Power On/Off Switch - A two position switch mounted externally on the back of the reader, used to switch the mains power to the reader On or Off.

Mode Switch - A three position switch mounted externally on the back of the reader, used to select the mode of operation of the reader:

OFF	The reader is inoperative.
LOCAL	The reader is operative under the control of the operator.
REMOTE	The reader is operative under the control of the system.

Reset Switch - A push button switch mounted externally on the front of the reader, used to start or restart the reader in certain modes.

Stop Switch - A push button switch mounted externally on the front of the reader, used by the operator to stop the reader as required.

Apart from the main controls, lamps are provided to indicate the state of the reader and other switches are provided for the testing of the lamp and the setting of the reader for automatic or manual shutdown when necessary.

Basic Specifications

Operating Speed	- 300 cards per minute.
Size	- Width 58.6 cm, height 41.2 cm,
	- Depth 45.7 cm.
Weight	- 34.4 Kilograms.
Card Specifications	- Standard 80 column card.
Power	- 1650 VA starting, 600 VA running.
Operating Temperature	- 15 - 25°C Limits imposed by cards.
Relative Humidity	- 50 - 70%.

P809-002 Matrix Line Printer

Figure 17.6 shows the P809-002 matrix line printer.

Figure 17.6

The P809-002 matrix line printer provides the system with the ability to produce a printed output at a rate of up to 200, 132 column lines per minute on standard fan folded paper, with a character set of 72 characters. Where necessary an output can be to a preset format and adjustment is possible to accomodate a paper width between 100 and 440 mm.

The carriage is a shuttling bar mounted on a support which moves in the horizontal plane between two side plates.

The printer is a free standing unit and includes its own power supply.

Connection to the system

Connection to the system may be via the programmed channel or input/output processor channel.

Main Controls

POWER ON - A pushbutton indicator holding switch mounted externally used to switch the main power to the printer on and when pressed again, off.

START/STOP - A pushbutton momentary indicator switch mounted externally. When pressed the indicator is lit and the printer is operational. When pressed again the indicator light is extinguished and the operator can use the TOP OF FORM and SINGLE LINE pushbuttons.

TOP OF FORM - A pushbutton momentary switch mounted externally whose action is inhibited when the START/STOP button is lit. When pressed in STOP mode the paper is advanced to the next top of form position.

SINGLE LINE - A pushbutton momentary switch mounted externally whose action is inhibited when the START/STOP button is lit. This pushbutton allows to advance the paper one line.

ERROR - An indicator which is lit when an error condition occurs.

Basic Specifications

Operating Speed	- 200 lines per minute.
Line Length	- 132 characters.
Size	- Width 700 mm, height 800 mm,
	- Depth 460 mm.
Weight	- approx. 80 Kilogram.
Paper Specification	- Single Copy 15 lb bond min. Multiple Copy up to 5 parts 11 lb bond with interleaved carbon. Paper width 100 - 440 mm.
Power Consumption	- 300 VA.
Operating Temperature	- 10 - 40°C.
Relative Humidity	- 20 - 80%.

P811-001 Line Printer
Figure 17.7 shows the P811-001 line printer.

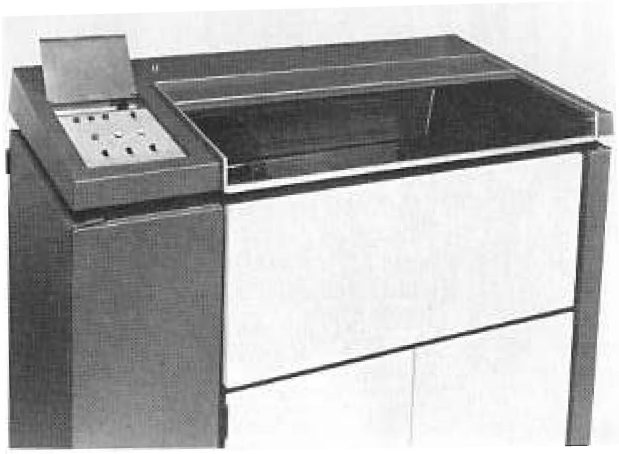


Figure 17.7

The P811-001 line printer provides the system with the ability to produce a printed output at a rate of up to 245, 132 character, lines per minute on standard fan folded paper. Where necessary an output can be to a preset format and adjustment is possible to accomodate various widths of paper, either single or multiple copies being available.

The printer is of the drum type with a character set of 64 characters, is free standing, and includes its own power supply.

Connection to the System
Connection to the system may be via the programmed or an input/output processor channel.

Main Controls
Power On/Off Switch - A two position switch mounted externally on the top of the printer, used to switch tha main power to the printer On or Off.

On Line/Off Line Switch - A two position switch mounted externally on the top of the printer, used to switch the printer On or Off line from the system.

Paper Step Switch - A two position switch mounted externally on the top panel of the printer, spring loaded to the off position, and operative when the printer is off line. When depressed it causes the paper to be advanced by one line.

Top of Form Switch - A two position switch mounted externally on the top panel of the printer, spring loaded to the off position, and operative when the printer is off line. When depressed it causes the paper to be advanced to the top of form position.

Basic Specifications

Operating Speed	- 245 lines per minute.
Line Length	- 132 characters.
Size	- Width 1232 mm, height 1168 mm, Depth 622 mm.
Weight	- 272 Kilogram.
Paper Specification	- Single Copy, 15 lb bond min. Multiple Copy up to 6 parts 12 lb bond with interleaved carbon. paper width, 102-251 mm.
Power	- 500 VA.
Operating Temperature	- 10 - 43°C.
Relative Humidity	- 30 - 80%.

P812-001 Line Printer

In all respects except basic specifications the P812-001 printer is the same as the P811-001 printer.

Basic Specifications

Operating Speed	- 670 lines per minute.
Line Length	- 132 characters.
Size	- Width 1232 mm, height 1168 mm, Depth 622 mm.
Weight	- 362 Kilogram.
Paper Specification	- Single Copy, 15 lb bond min. Multiple Copy up to 6 parts 12 lb bond with interleaved carbon. paper width, 102 - 251 mm.
Power	- 500 VA.
Operating Temperature	- 10 - 43°C.
Relative Humidity	- 30 - 80%.

P831-002 Magnetic Tape Unit

Figure 17.8 shows the P831-002 magnetic tape unit.

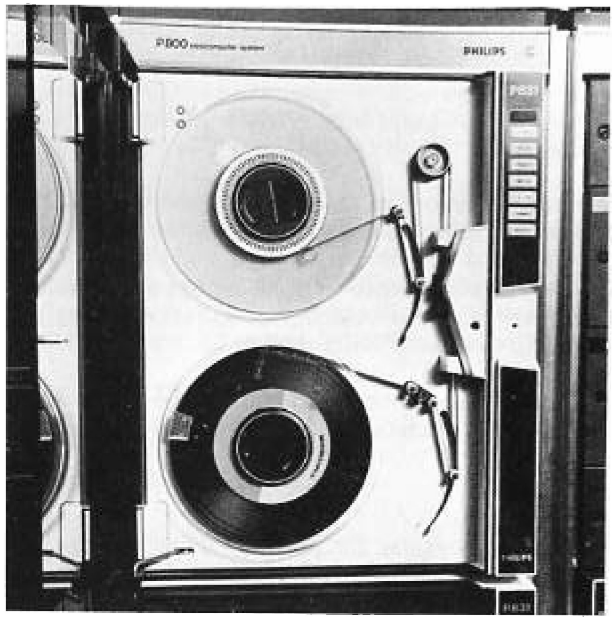


Figure 17.8

The P831-002 magnetic tape unit provides the system with the ability to transfer data to or from magnetic tape at a rate of up to 20k characters per second. Recording density is 800 bits per inch and a NZRI method of recording data in 9 track format is used. Tape handling is via a servo controlled drive unit and two 10.5 inch reels at a tape speed of 25 inches per second. The unit incorporates its own power supply.

Connection to the System

Connection to the system must be made via an appropriate tape formatter which is in turn connected to the system via an input/output processor channel. Upto 4 magnetic tape units may be connected to, and controlled via, a single formatter unit.

Mounting

The tape unit is assembled for mounting in a standard 19" rack, fitting being by hinges to the front of the rack frame. The unit may be fitted into either the basic or an extension cabinet.

Main Controls
All the main controls are situated externally on the front panel of the unit and include indicators within the push button switches.

Power - Used to switch the main power to the unit On or Off and to indicate power on.

Load - When initially pressed the switch causes the energising of the servo mechanism and the tape is wound taught. When pressed again the tape is advanced to the load point.

On Line - Alternate operations of the switch cause the unit to be switched on and off line respectively, the indicator is lit when the unit is on line.

White Enable - Alternate operations of the switch cause the unit to be switched between the Read/Write and the Read Only mode of operation, the indicators is lit when the unit is in the Read/Write mode.

Other switches are provided to operate the unit in the Off line mode giving the operator the facility to run the tape forward or backwards and rewind the tape as necessary.

Basic Specifications

Operating Speed	- Tape, 25" per second, 800 bits per in. Transfer, 20k characters per second.
Size	- Width 483 mm, height 622 mm, Depth 318 mm.
Weight	- 38 Kilograms.
Tape Specification	- Width 12.7 mm, Thickness 0.038 mm, Length 731 m, 267 mm reels.
Power	- 300 VA.
Operating Temperature	- 2 - 35°C
Relative Humidity	- 15 - 95%.
Size	- Width 483 mm, height 89 mm, Depth 508 mm.
Weight	- 11 Kilograms.
Power	- 100 VA.
Operating Temperature	- 2 - 50°C.
Relative Humidity	- 10 - 95%.

P831-004 Magnetic Tape Unit
This unit provides the system with the same facilities as the P831-002 Magnetic Tape Unit but with increased tape drive speed and transfer rate. In all other respects the respective units are the same.

Operating Speed Tape, 45" per second
800 bits per in.
Transfer, 36k characters per second.

P831-010 Tape Formatter
The P831-010 tape formatter provides the necessary control and timing to connect up to 4 P831-002 tape units to the system. It contains its own power supply and will normally be mounted in the back of the same rack as one of the drive units it controls. It is fitted with a power On/Off switch and indicator which will normally be accessible when the rear of the cabinet containing the unit is open.

P831-020 Tape Formatter
The P831-020 tape formatter provides the necessary control and timing to connect up to 4 P831-004 tape units to the system. It contains its own power supply and will normally be mounted in the back of the same racks as one of the drive units it controls. It is fitted with a power On/Off switch and indicator which normally is accessible when the rear of the cabinet containing the unit is open.

P831-006 Magnetic Tape Unit
This unit provides the system with the same facilities as the P831-002 Magnetic Tape Unit but with increased tape drive speed and transfer rate. In all other respects the respective units are the same.

Operating Speed Tape, 37.5" per second.
1600 bits per in.
Transfer, 60k characters per second.

P831-030 Tape Formatter
The P831-030 tape formatter provides the necessary control and timing to connect up to 4 P831-006 tape units to the system. It contains its own power supply and will normally be mounted in the back of the same rack as one of the drive units it controls. It is fitted with a power On/Off switch and indicator which will normally be accessible when the rear of the cabinet containing the unit is open.

P833-001 Cassette Drive Unit
Figure 17.9 shows the P833-001 cassette drive unit.

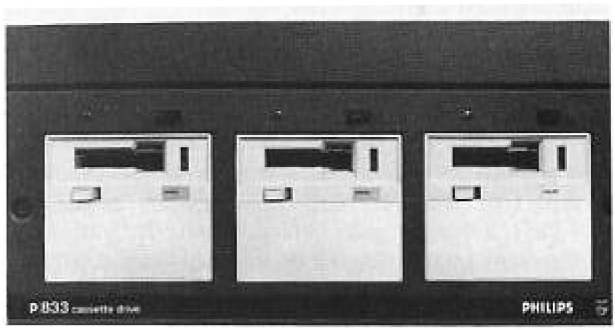


Figure 17.9

The P833-001 cassette tape unit provides the system with the ability to transfer data to or from cassette tape at a transfer rate of up to 750 characters per second.

The tape unit drives the cassette tape at a speed of 7.5 inches per second and data are recorded or read serially at a density of 800 bits per inch on two separate tracks.

Connection to the System
Connection to the system may be via the programmed or input/output processor channel and up to 3 units may be controlled by a single control unit.

Mounting
The unit is assembled for mounting into a chassis which is itself designed for mounting in a standard 19" rack. Up to 3 units may be mounted into one chassis and each chassis contains a power supply and control unit to power and handle the units fitted into it.

Main Controls
Only one external control is fitted to the front of the unit, the Retrieval Knob, this knob is depressed to release and enable removal of a cassette. The knob is locked and unable to be depressed when a unit is in operation. Indicators on the front of the unit show when the unit is locked and the approximate amount of tape used at any one point.

Basic Specifications

Operating Speed	- Tape 7.5" per second, 800 bits per in. Transfer 750 characters per second.
Size	- Width 123 mm, Height 139 mm, Depth 280 mm.
Weight	- 3.5 Kilograms.
Tape Specification	- Width 3.81 mm, Length 86 m.
Power	- 24 V, 0.85A steady.
Operating Temperature	- 0 - 50°C.
Relative Humidity	- 5 -95%.

P833-152 Cassette Tape Controller

The P833-152 Cassette Tape Controller provides mounting facilities for up to 3 P833-001 cassette units and includes its own 24V power supply unit and control circuits.

Basic Specifications

Size	- Width 483 mm, height 178 mm, Depth 617 mm.
Weight	- 15 Kilograms.
Power	- 80 VA.
Operating Temperature	- 0 - 50°C.
Relative Humidity	- 5 - 95%.

MAGNETIC DISC EQUIPMENT

P824-002 Moving Head Disc Unit

Figure 17.10 shows the P824-002 moving head disc unit.

Figure 17.10

This moving head disc unit provides the system with the ability to transfer data to or from a magnetic disc cartridge at a rate of up to 312k characters per second after initial access to the disc area required. Head positioning is carried out by an electro-mechanical mechanism with a positive positioning detent, the avarage positioning time being only 30 ms. Data are recorded on or read from the disc serially, 78k characters (or bytes) per track being possible. Each surface of the disc contains 200 tracks providing an overall capacity of 2.7M characters. A second, fixed disc is incorporated within the unit. The moving heads for this are combined within the overall head mechanism and thus the capacity, transfer rate and access time are all the same as for the exchangeable cartridge, overall capacity of the unit with the fixed disc being 5.4M characters. Apart from the drive and head position mechanism the unit contains its own power supply and all the necessary control logic for correct operation.

The exchangeable recording disc is a Philips 14" mono disc cartridge, P842-100, and is fully compatible with the IBM 5440 type of cartridge with 16 sectors.

Connection to the System
Connection to the system is via an input/output processor.

Mounting
The complete unit is assembled for mounting within a standard 19" rack by means of mounting kit P849-039 and fitting may be in either the basic or an extension cabinet. The drive unit is slide mounted within the rack to enable cartridge changing and engineering maintenance.

Main Controls
All the main controls are mounted externally on the front panel of the unit and incorporate their own indicators.

Power On/Off Indicator – Is lit when the power is switched on.

Start/Stop Switch – A push button switch used to start and stop the drive to the disc.

Apart from the main controls indicator lamps are fitted on the front panel to indicate Cartridge Exchange and certain fault conditions.

Basic Specifications

Operating Speed	– Disc rotation, 2400 r.p.m.
	– Transfer, 312k characters per second.
Average Latency	– 12.5 msec.
Average Access time	– 33 ± 2 msec.
Size, Drive Unit	– Width 480 mm, Height 262 mm (3U) Depth, 752 mm.
Weight, Drive Unit	– 60 Kilograms.
Power	– 150 VA running (600 VA starting).
Operating Temperature	– 10 - 35°C.
Relative Humidity	– 20 - 80%.

P825-007 Moving Head Disc Unit
Figure 17.11 shows the P825-007 moving head disc unit.

Figure 17.11

This moving head disc unit provides the system with a mass memory random access device with an exchangeable 5-disc cartridge (P825-100). The cartridge is driven by a ½ hp spindle motor and is placed on the spindle by opening the hinged shroud cover on top of the unit.
The disc pack contains 5 recordable surfaces each one having 411 tracks of which 7 are spare ones. Data are recorded on or read from the disc serially. Recording is possible up to 21,5k characters (bytes) per track. The overall capacity of the disc pack is 40M bytes.
Head positioning is carried out by a closed loop proportional servo system. The carriage is driven by a voice coil linear actuator with position feedback provided from the disc pack servo service.
The average positioning time is 30 ms.

Connection to System
Connection to the system is via an input/output processor.

Main Controls

All the main controls are mounted externally on the unit's front panel.

Start Switch to start and stop the unit. It is lit when pressed.

Ready Indicator which is lit when the pack is up to speed, the heads are loaded and no fault condition exists.

Fault Lights when a fault condition occurs. When pressed in that case the fault flip-flop is cleared.

Apart from the main controls on the front panel two switches are mounted on the back panel to connect the mains and the power supply unit.

Basic Specifications

Operating Speed	- Disc rotation, 3600 r.p.m.
Average Latency	- 8.33 msec.
Average Access time	- 30 msec.
Height	- 34.0 in. (864 mm)
Depth	- 34.0 in. (864 mm)
Width	- 19.0 in. (483 mm)
Weight	- 100 Kilograms.
Power	- 150 VA (standby), 620 VA (operation).
Operating temperature	- 15 - 32°C.
Relative Humidity	- 20 - 80%.
Data Transfer Rate	- 1,2M char./sec.
Disc Diameter	- 14 inches.
No of discs	- 5 (3 data and 2 cover plates).
Servo Service	- 1
Recording Surfaces	- 5
Tracks per Surface	- 404 plus 7 spares.
Tracks spacing	- 0.0052 inch nominal.
No, of Servo heads	- 1
No, of Recording heads	- 5

P818-001 Display

Figure 17.12 shows the P818-001 display.

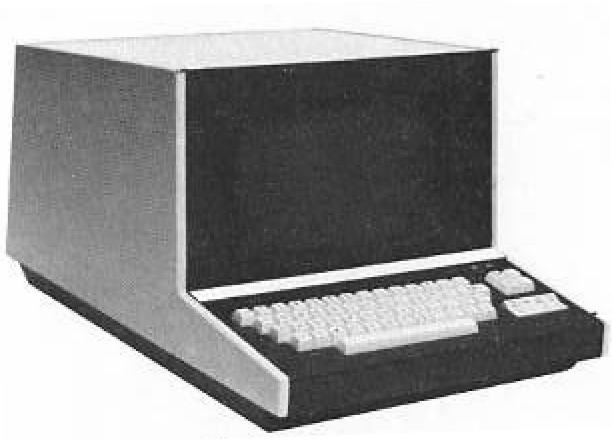


Figure 17.12

The P818-001 display provides the system with a table-top terminal which displays its information on a 12" screen size, 80 characters per line. The attached keyboard allows 64 ASCII alphanumerics and symbols. The number of lines displayed on the screen is 24 lines.

Connection to the System

Connection to the system is done via the current loop interface implemented on the AMA8C.

Main Controls

Power On/Off switch – An external two position switch used by the operator to switch the mains power to the display on or off.

LINE RDY - indicator which is lit red when the display is operational.

PARITY ERROR - lights red in case of a parity error.

PARITY RESET	- springloaded pushbutton which must be pressed when a parity error occurred.
RESET	- springloaded pushbutton. When pressed all internal functions are reset and the screen is cleared.
ON LINE/OFF LINE	- rocker switch. ON LINE - the display is connected to the system. OFF LINE - the display is operational but not connected to the system.
TPWR/TTY	- rocker switch. TPWR - lower case and upper case facility. TTY - upper case facility.
HIGH RATE/LOW RATE	- rocker switch. Its use is determined at installation time.
FULL DUP/HALF DUP	- rocker switch. FULL DUP - full duplex. Used for echoplex technique where the computer echoes back each character for display on the screen. - HALF DUP - half duplex. Characters are directly displayed on the screen.
Contrast	- thumbwheel to adjust the brightness of the characters on the screen.

Basic Specifications

No of lines	- 24
No of char. per line	- 80.
Transmission rate	- 110 to 9600 bauds.
Transmission mode	- asynchronous.
Parity selection	- by switch: odd, even, none.
Interface	- current loop.
Size	- Length 381 mm, Height 292 mm, Depth 508 mm.
Weight	- approx. 17.4 kg.
Power	- 200 VA.
Operating Temperature	- 10 - 40°C.
Relative Humidity	- 10 - 90%.

P818-002 Display

This display provides the same functions as the P818-001 but it has a V24 interface.

Connection to the system

Connection to the system may be done via the integrated serial control unit or the P845-040/002 Serial Control Unit or via Data Communication interfaces such as ALCU2, ALCU4 or the AMA8A.

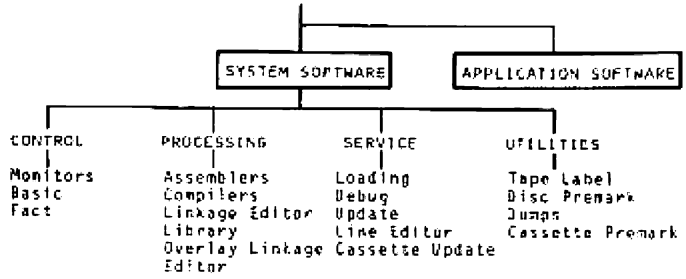


Figure 18.1 Standard System Software and Application Software

Software consists of two main divisions, as shown by figure 18.1. The application software shown is not further divided as this represents the programs a user writes to carry out his processing requirements, these of course will vary considerably from user to user. System software consists of all those programs a user may employ to efficiently produce and execute his application software and is made up of the control, processing, service and utility programs shown by figure 18.1. Full descriptions of the available system software are covered in the appropriate software manuals and therefore only a brief description of the software is given here.

All software may be of a modular construction, and in the case of the monitors, a user may select the modules he requires at the time of generating the system. The main advantages offered by modular programming are:

1. Modules may be written in different source languages and by different programmers thus enabling an efficient and speedy solution to any problem.
2. Common routines may be written and held for use by a number of programs.
3. Testing, error detection and correction procedures are simplified.
4. Updating is simplified.

Figure 18.2 shows the method of modular construction used within the monitors as an example of modular programming. Each monitor may be assembled from only those modules it requires.

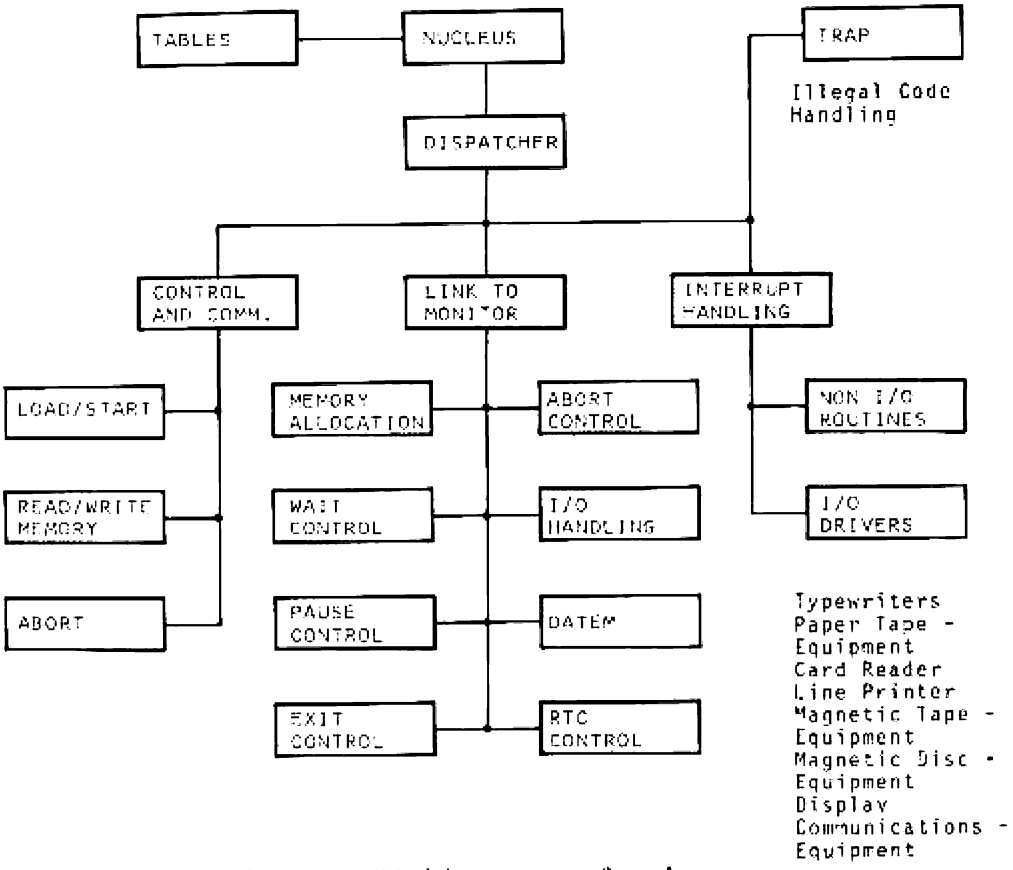


Figure 18.2 Modular structure of monitor

System software is available in stand alone software or monitor controlled versions. Stand alone programs are completely self contained and thus do not require to use any of the facilities available from the monitors, whilst monitor controlled programs are available for paper tape, cassette tape and disc oriented systems. Figures 18.3 to 18.9 show the standard system software configurations.

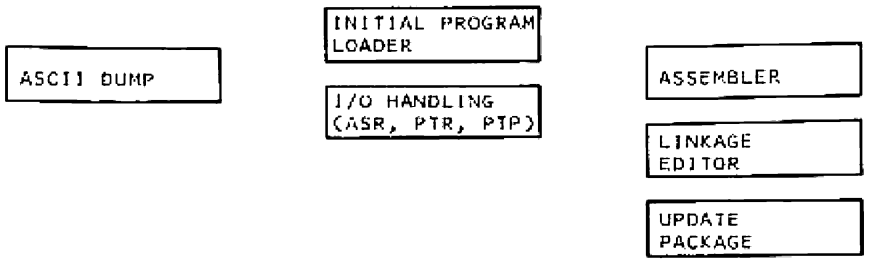


Figure 18.3 Stand Alone Software

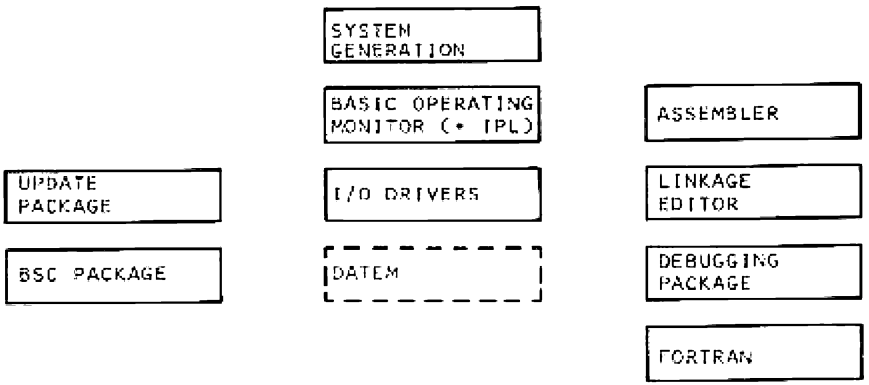


Figure 18.4 Software for Basic Operating System

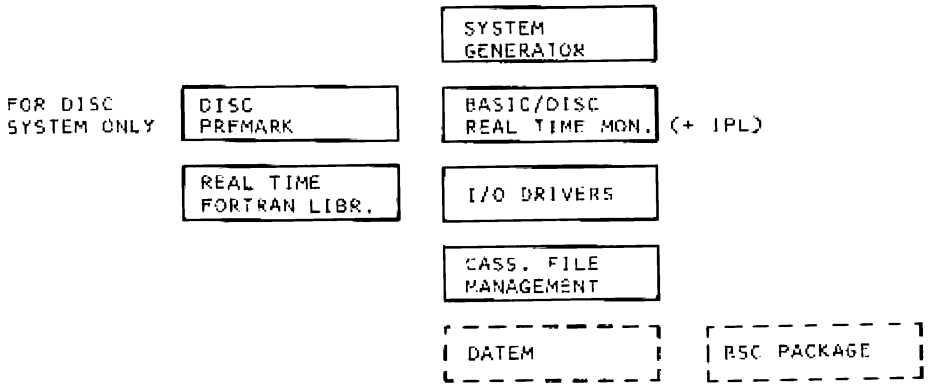


Figure 18.5 Software for Basic and Disc Real Time System

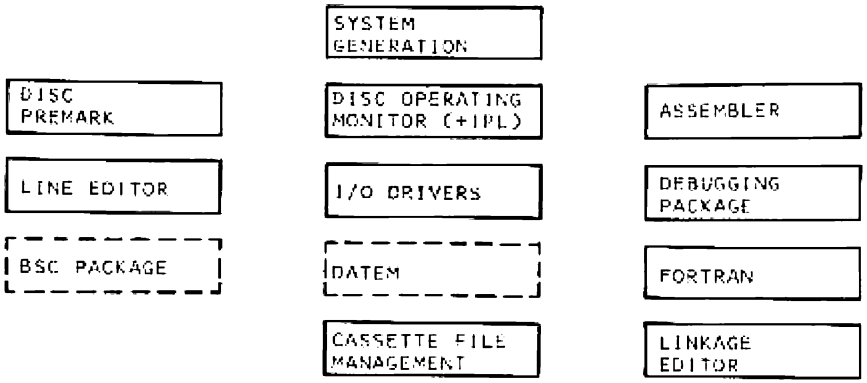


Figure 18.6 Software for Disc Operating System

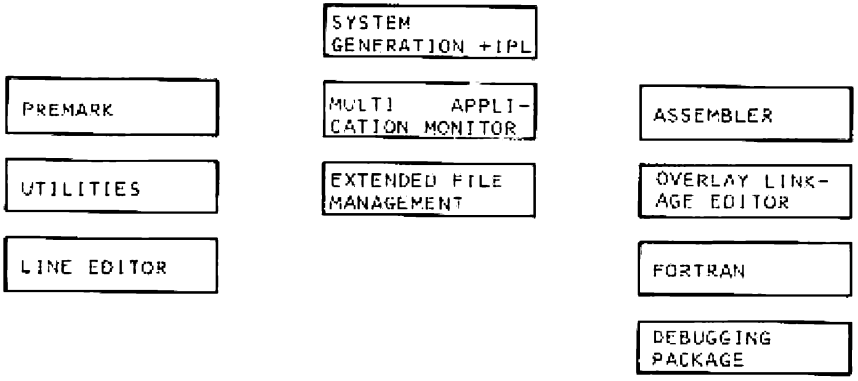


Figure 18.7 Software for Multi Application System

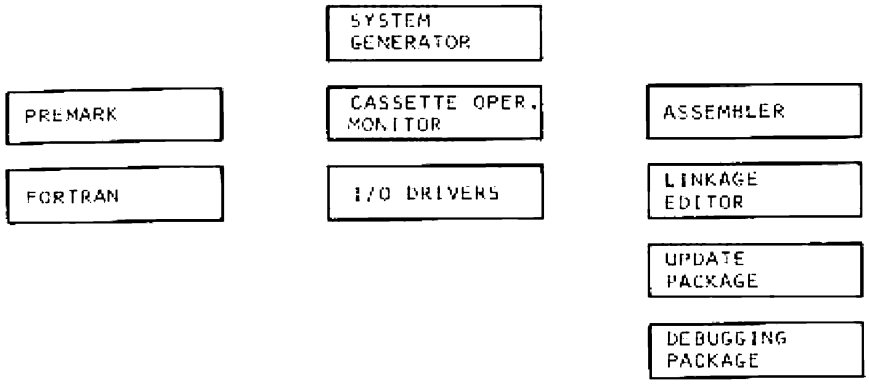


Figure 18.8 Software for Cassette Operating System

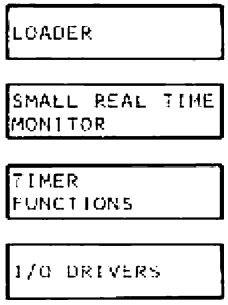


Figure 18.9 Software for Small Real Time System

CONTROL PROGRAMS

The loading, preparation and supervised execution of application and certain system software may be handled by control programs, known within system software as monitors. Being of modular construction a user may select only those modules which he needs when generating his system, and if necessary expand the monitor facilities as and when the hardware system is enhanced.

There are seven monitors currently available, one for each of the software configurations that require a control program. The monitors available are:

1. Basic Operating Monitor.
2. Basic Real Time Monitor.
3. Disc Operating Monitor.
4. Disc Real Time Monitor.
5. Cassette Operating Monitor.
6. Small Real Time Monitor.
7. Multi Application Monitor.

Basic Operating Monitor

The basic operating monitor provides the system with the ability to handle controlled system software and application software on a non-real time basis. The monitor is paper tape orientated in its standard form but may be extended to handle other peripherals as necessary. The use of the systems interrupt handling and a facility of scheduled labelling, which allows for the immediate commencement of a specified routine on completion of a specified input/output process, enables the monitor to exercise control of programs speedily and efficiently. The normal use of the basic operating monitor is to provide the necessary control when a user is producing and testing applications software prior to the use of such software in a real time environment.

The minimum configuration requirements for operating with the basic operating monitor are 8k words of memory and an operator's typewriter with associated paper tape equipment, the monitor itself occupying between 3k and 5k of central memory. In the smallest case only the operator's ASR and associated paper tape equipment together with the necessary program control modules may be specified.

Basic Real Time Monitor

The basic real time monitor provides the system with the ability to handle controlled application and certain system software on a real time basis. This facility is based on a use of time sharing, or slicing, between different programs which are running at the same software level; and a system of software and hardware levels to efficiently handle the input/output requirements of a number of programs. All the facilities available to the Basic Operating Monitor, together with

control facilities necessary for connecting programs to software levels and timers, and the organization of the use of common subroutines and buffer areas, are available to the Basic Real Time Monitor.

The minimum configuration requirements for operating with the basic real time monitor are 8k words of memory and an operator's typewriter with associated paper tape or cassette tape equipment, the monitor itself occupying upwards of 3k of memory. In the smallest case only the operator's ASR and associated paper tape equipment, together with the real time clock and other necessary program control modules may be specified.

Disc Operating Monitor
The disc operating monitor provides a disc orientated system with all the facilities available to the Basic Operating Monitor, and in addition provides the necessary control for the secure allocation and utilization of both user and system files within any system. Both system and user programs that are to be used are held on a disc within the system, and are called into central memory and executed as required. The running of user programs or the updating of system information is carried out during a session, which must be commenced by a specific user identification, and only the files of the declared user may be accessed for writing during any specific session, the files of other users may however be read. All user identifications including the system are catalogued and each identification refers to a library of files which is only accessible via the catalogue and under monitor control, thus ensuring security of data.

Throughout a session processing is carried out within temporary files but at any time during the session a user may retain files by keeping them within his library.

The minimum configuration requirements for operating with the disc operating monitor are 16k words of central memory, an operator's typewriter and one disc.

Disc Real Time Monitor
The disc real time monitor provides a disc orientated system with all the facilities of the basic real time monitor and the disc facilities of the disc operating monitor, in addition the monitor is able to allocate central memory to running programs which have been loaded from the disc and where necessary restore programs to the disc to make central memory space available for higher priority programs.

The minimum configuration requirements for operating with the disc real time monitor are 8k words of central memory, an operator's typewriter, and one disc.

This Monitor may be extended with the Extended File Management Package.

Cassette Operating Monitor
The Cassette Operating Monitor (COM) is a monitor which handles one program at a time and may be considered as a cassette tape oriented program development tool.

At system generation time, the user creates his own system cassette, on which the monitor is the first program, preceded by an Initial Program Loader (IPL). The monitor is loaded by this IPL, which is loaded by bootstrap according to the data switches on the CPU control panel.
Then the user program or a processor is loaded. If the operator communication package is included and used for this purpose, separate commands must be given to load and start. If the cassette file management package is included, one single command will be enough to seek, load and start a program.
The cassette file management (CFM) package is used to handle I/O operations on cassette tape according to certain ECMA standards, one of which is the type of labelling of the tape. The CFM will accept three types of increasing labelling complexity: Basic, Compact and Extended. The system software is given in Compact type of labelling, which allows the handling by the COM of single-track, multi-track and multi-volume files as well as multi-file tracks and volumes. Files are preceded by headers and followed by End of File records, tracks end with End-Of-Track records, volumes (i.e. one complete cassette) with End-Of-Volume records. This is all handled automatically by the cassette file management package; it includes a number of control commands by means of which the user can write or search headers, run a program, etc.
The monitor itself handles the standard interrupt signals, controls I/O operations and executes functions requested by the used in his program by means of monitor requests, e.g. requesting and releasing temporary bufferspace in memory, waiting for events, making exits, etc.
The monitor modules are centered around a dispatcher, which determines on the basis of interrupt signals and priority levels which routine or program must be executed.
Although the COM is designed to handle one program at a time, a form of multi-tasking can be achieved by using scheduled label routines. These routines are attached to the specification of a monitor request and enable a program to run concurrently with, for example, an I/O operation.

Although the COM is cassette tape oriented, other peripherals can be handled as well. This can all be determined by the user at system generation time.

Small Real Time Monitor
The Small Real Time Monitor is developed for dedicated computer applications requiring a small and fast monitor. The monitor is paper tape oriented.

Included in the monitor are timer functions for control of the user programs. Fourteen software priority levels allow multiprogramming between user tasks, one or more programs may be connected to the same level.
The monitor is upward compatible with the Basic Real Time Monitor.

Multi Application Monitor
The Multi Application Monitor is particularly well suited for a number of applications:

- multi tasking applications where a large memory size (up to 128k) allows more resident programs or several transient programs to be in core, improving response time and overall performances.
- foreground/background applications where program debugging can be made concurrently with a real-time process.
- data communication applications where many buffers and tables have to be resident due to fast access time.

The Multi Application Monitor is a disc oriented monitor and has a clear open ended structure; at each application corresponds a sub-machine defined by:
- several priority levels,
- several allocated or shared peripheral devices (spooling),
- several memory partitions,
- several disk file libraries.

More than one multi-tasking or real-time sub-machine exist; programs can be connected to a real-time clock or timer, several disk resident programs can be in memory at the same time (multi-transient areas).
A batch processing sub-machine supports other system components including Assembler, Overlay Linkage Editor, Full Fortran Compiler, Line Editor etc. This sub-machine is specially oriented towards program development. Each sub-machine and the monitor itself are individually protected. The Monitor can be extended with the Extended Disc File Management Package which adds to the existing system data base facilities with direct and sequential access, variable length data records, indexed organisation, file protection and on-line updating.

A set of operator commands is available e.g. to create or suppress a sub-machine, to allocate or deallocate memory for a sub-machine, to assign peripheral devices or files, to start or stop tasks inside sub-machines.

DATEM

DATEM is a datacommunication monitor extension to the Basic Operating Monitors, the Disc Operating Monitor and the Basic and Disc Real Time Monitors.
It provides the system with basic data communication facilities. The standard features of the monitors remain available for the system. The extension takes care of the following functions in a data communication configuration:
- Connection to the line (leased lines and switched lines).
- Read or write data.
- Error control.
- Time-out control.
- Data control (wait for data, polling and selecting, stop the transmission on detection of special characters).

BSC

BSC is the Binary Synchronous Communication line procedure package which may be used for synchronous communication. It handles the line control of the transmitting and receiving stations.

PROCESSING PROGRAMS

These programs consist of assemblers, compilers, linkage editor and overlay editor available to a user for the production of his application software. Various versions of the programs are possible to meet the requirements of different systems and in most cases a stand alone and a monitor controlled version are available.

Assemblers

The assemblers convert source modules written in assembly language into object modules suitable for linking to other object modules or for loading and execution. Each line of a source module is written in assembly language and represents one central processor instruction, word or block of data or directive, to control the assembly process. Additional features available include error reporting and recovery, assembly listing and the selection of the peripheral devices to be used during processing.
Two versions of the assembler exist: a stand alone version and a monitor control version (either Basic or Disc oriented).

FORTRAN Compilers

The FORTRAN compilers translate FORTRAN source programs into object modules to be processed by the Linkage Editor or Overlay Editor with the Mathematical Library. The result of the editing process is a self-contained executable program which can run under control of the monitor. The compilers are self-initializing and do not require reloading between successive compilations.
The Full FORTRAN compiler produces object modules in interpretive code, which is translated into executable machine code instructions at run time by the object code interpreter routine linked to the FORTRAN program. The High-Speed FORTRAN Compiler accepts the same source language as the Full FORTRAN compiler with some extension for disc random access, and produces machine code object directly.
For systems controlled by the Basic Operating Monitor a transcoder is available to translate interpretive object modules into directly executable machine code.
The Real Time FORTRAN system is a system in which user written FORTRAN programs run under control of a real time monitor. The Real Time FORTRAN library consists of a set of routines which are called by the FORTRAN program whenever their use is required.

Linkage Editor
The Linkage Editor is available for the Stand Alone, Basic and Disc Operating Systems providing the facility to link separate object modules either for direct loading and execution or for output (BOS only), to be loaded later or used within a further linkage process. By linking, all the advantages of modular programming are easily available. Modules which are to be linked are written containing specified external references and entry points to be used during linkage, and the control of the linkage process by the operator, allows for the selection of the peripherals and mode to be used during processing.
In addition the program provides the listing of a map reports errors during processing.

Overlay Linkage Editor
This processor runs under control of the Multi Application Monitor. It applies for large programs which cannot fit in the available partition. The Overlay Linkage Editor produces from a set of object modules a segmented program organised in an overlay structure which is transparent to the user. It satisfies all the external references and produces calling sequences for loading the different segments. In case of one segment the processor can also be used as a simple Linkage Editor.

After processing a load module is produced recorded on a temporary load file. This load module may be executed and/or kept in library.
A number of options may be typed in e.g. to specify an absolute loading address, the start address of a common area or the specification which library will be scanned, and some information required by the Debugging Processor.

SERVICE AND UTILITY PROGRAMS

The programs within these groups provide the user with all the facilities required to set up, run, and maintain the system apart from the tasks of initial program production.

Debugging
Debugging programs are available to enable rapid error detection within program modules, and to provide the programmer with the ability to stop a program at specific points so that the contents of memory and/or registers may be checked or altered as necessary.

Update
An update program is available for stand alone systems or for use with BOM providing the facility to insert or delete lines or modules at source level and to insert or delete modules at object level. Initial control of the update program is carried out by the operator or programmer from the operator's typewriter, and various options exist to enable the system's other peripheral devices to be used during the complete update process.

The minimum configuration requirements for operating the update facility are 8k words of central memory, an operator's typewriter, and high speed paper tape reader and punch.

Line Editor
The line editor, available for use within the disc operating system configuration, provides all the facilities of the Update Package and an additional facility to enable the alteration of a specified character string wherever such a string appears in a module.

Cassette Update
The Cassette Update allows the user of the Cassette Operating System to update his files, libraries and sources or object modules.
The Update Package at file level, module level or line level and comprises functions as copy, skip, delete, insert and list.
Editing is done by means of control commands of which some pertain to a certain level. It is possible to switch from one level to another during an edit run.

Utility Programs
These programs are used by the user during the setting up of the systems files, and where necessary during the normal running of the system to provide the marking and labelling facilities required by certain peripherals and the information required by certain processes.

BASIC

BASIC is a stand alone system for compiling and executing programs written in the BASIC (Beginners All-purpose Symbolic Instruction Code) language. The BASIC system consists of a monitor and a compiler. It is a conversational system, on which up to 16 users can work simultaneously from terminals. A time-slicing mechanism, which divides processing time in equal parts over all terminals, makes the system appear to each user as occupied by him alone. The actual execution of programs is done by incremental compilation: each statement is compiled separately, and executed immediately. The generated object code is not stored, to economize on memory space.
The system is completely memory resident. It needs a high speed paper tape reader, an ASR typewriter for each user, and depending on the number of users 8 to 20k words of memory.

FACT

FACT, which stands for Facility for Automation Control and Test, is a software system operating as a programmable controller, able to perform the control functions generally required in control and automation projects, such as production control, traffic control, functional test of integrated circuits and printed circuit boards, and various types of security systems.

The control functions are provided by FACT user programs, written in simple instruction statements. The FACT system translates the instructions into control signals for the process, and transmits signals from the process to the control program.

The FACT system is memory resident, and occupies only 0.5k memory words. An Update processor of 0.5k memory words is available to produce and change FACT user programs.

Appendix 1 Peripheral Manufacturers

P841	Operator's Typewriter	- Teletype Corporation
P842	Matrix Printer	- Philips Terminal Systems
P801/802	Paper Tape Reader	- Digitronics Corporation
P803	Paper Tape Punch	- Facit
P809	Matrix Line Printer	- Philips
P811/812	Line Printers	- Data Products
P806	Card Reader	- Documentation
P831	Magnetic Tape Drive	- PERTEC
P833	Cassette Tape Drive	- Philips
P824	Moving Head Disc	- Philips
P825	Moving Head Disc	- Control Data
P818	Visual Display Unit	- Hazeltine

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P803	Paper Tape Punch	- Facit
P809	Matrix Line Printer	- Philips
P811/812	Line Printers	- Data Products
P806	Card Reader	- Documentation
P831	Magnetic Tape Drive	- PERTEC
P833	Cassette Tape Drive	- Philips
P824	Moving Head Disc	- Philips
P825	Moving Head Disc	- Control Data
P818	Visual Display Unit	- Hazeltine