

# Fix Drive

## TABLE OF CONTENTS

	Page
<b>1.0 Introduction</b>	
1.1 General Description	1
1.2 Specification Summary	2
1.2.1 Physical Specifications	2
1.2.2 Reliability Specifications	2
1.2.3 Performance Specifications	3
1.2.4 Functional Specifications	3
<b>2.0 Functional Characteristics</b>	
2.1 General Operation	3
2.2 Read/Write and Control Electronics	3
2.3 Drive Mechanism	4
2.4 Air Filtration System	4
2.5 Positioning Mechanism	4
2.6 Read/Write Heads and Discs	8
<b>3.0 Functional Operations</b>	
3.1 Power Sequencing	8
3.2 Drive Selection	8
3.3 Track Accessing	8
3.4 Head Selection	8
3.5 Read Operation	10
3.6 Write Operation	10
<b>4.0 Electrical Interface</b>	10
4.1 Control Input Lines	15
4.1.1 Reduced Write Current	16
4.1.2 Write Gate	16
4.1.3 Head Select 2 <sup>0</sup> and 2 <sup>1</sup>	16
4.1.4 Direction In	16

4.1.5 Step	16	7.3 Gap 3	35
4.1.6 Drive Select 1-4	19	7.4 Gap 4	35
4.2 Control Output Lines	19	7.5 Sector Interleaving	35
4.2.1 Seek Complete	19	7.6 Defective Sector Flags	35
4.2.2 Track 0	19	<b>Figures</b>	
4.2.3 Write Fault	19	1 Air Filtration System	5-6
4.2.4 Index	20	2 Positioning Mechanism	7
4.2.5 Ready	20	3 Power Up Sequence	9
4.3 Data Transfer Lines	20	4 Control Signals	12
4.3.1 MFM Write Data	21	5 Data Signals	13
4.3.2 MFM Read Data	22	6 Typical Connection, 4 Drive System	14
4.3.3 Read/Write Timing	22	7 Control Signals Driver/Receiver Combination	15
4.4 Drive Selected	24	8 8A Step General Timing	17
4.5 Customer Options	24	8B Slow Seek Step Pulse Timing	17
4.5.1 "R" (Radial) Option	24	8C Algorithm Driven Seek	18
4.5.2 "D" (Defeat Recal) Operation	24	8D Buffered Seek	18
4.5.3 "H" (Half Step) Option	24	9 Index Timing	20
5.0 Physical Interface	26	10 Data Line Driver/Receiver Combination	21
5.1 J1/P1 Connector—Control Signals	27	11 Write Precompensation Patterns	22
5.2 J2/P2 Connector—Data Signals	28	12 Read/Write Data Timings	23
5.3 J3/P3 Connector—DC Power	28	13 Option Shunt Block	25
5.4 J4/P4 Frame Ground Connector	30	14 Interface Connector Physical Locations	26
6.0 Physical Specifications	30	15 J1 Connector Dimensions	27
6.1 Mounting Orientation	30	16 J2 Connector Dimensions	28
6.2 Mounting Holes	30	17 J3 Connector	28
6.3 Physical Dimensions	30	18 Mounting Physical Dimensions	31
6.4 Shipping Requirement	30	19 Overall Physical Dimensions	32
7.0 Track Format	33	20 Track Format As Shipped	34
7.1 Gap 1	33	21 "A1" Address Mark Byte	35
7.2 Gap 2	33		

## Tables

I	J1/P1 Connector Pin Assignments	11
II	J2/P2 Connector Pin Assignments	12
III	J3/P3 DC Connector Pin Assignments	12
IV	DC Power Requirements	29
V	Motor Start Current Requirements	29

## 1.0 Introduction

### 1.1 General Description:

The ST-506/412 disc drive is a random access storage device utilizing two non-removable 5 $\frac{1}{4}$  inch discs as storage media. Each disc surface employs one movable head to service 153/306 data tracks. The total formatted capacity of the four heads and surfaces is 5/10 megabytes (32 sectors per track, 256 bytes per sector, 612/1224 tracks).

Low cost and unit reliability are achieved through the use of a band actuator and open loop stepper head positioning mechanism. The inherent simplicity of mechanical construction and electronic controls allows maintenance free operation throughout the life of the drive. Both electronic PCB's are mounted outside the head disc assembly, allowing field serviceability.

Mechanical and contamination protection for the heads, actuator, and discs is provided by an impact resistant aluminum enclosure. A self-contained recirculating system supplies clean air through a 0.3 micron filter. A second port in the filter assembly allows pressure equalization with ambient air without chance of contamination. A patented spindle pump assures adequate air flow and uniform temperature distribution throughout the head and disc area. Thermal isolation of the stepper and spindle motor assemblies from the disc enclosure results in a very low temperature rise within the enclosure. This provides significantly greater off track margin and the ability to immediately perform read and write operations after power up with no thermal stabilization delay.

The ST-506/412 electrical interface is similar to Shugart Associates' SA1000 family of 8 inch fixed disc drives. ST-506/412 *size and mounting* are identical to the industry standard minifloppy disc drives, and they use the same DC voltages and connector. No AC power is required.

#### Key Features:

- ★ Storage Capacity of 6.38/12.76 megabytes unformatted, 5.0/10.0 megabytes formatted as shipped.
- ★ Same physical size and mounting as the minifloppy.
- ★ Same DC voltages as the minifloppy.
- ★ Band actuator and stepper motor head positioning.
- ★ 5.0 megabit/second transfer rate.
- ★ Simple floppy-like interface.
- ★ Same track capacity as a double density 8 inch floppy.

## 1.2 Specification Summary:

### 1.2.1 Physical Specifications:

#### Environmental Limits:

##### Ambient Temperature

Operating: 40° to 122°F (4° to 50°C)

Non-Operating: -40° to 140°F (-40° to 60°C)

##### Max Temperature Gradient

Operating: 18°F/hr. (10°C)

Non-operating: Below Condensation

Relative Humidity: 8 to 80% non-condensing

Max Wet Bulb: 78.8° (26°C)

##### Maximum Elevation

Operating: 10,000 ft.

Non-operating: -1000 to 30,000 ft.

##### Shock

Operating: 10G's

Non-operating: 20G's

#### DC Power Requirements

+12V ±5%, 1.8A typical, 4.5A maximum (at power on)

+5V ±5%, 7A typical, 1.0A maximum

+12V/+5V Maximum Ripple = 50mV P-P

#### Mechanical Dimensions:

Height ..... 3.25 inches

Width ..... 5.75 inches

Depth ..... 8.00 inches

Weight ..... 4.6 lbs. (2.1 kg)

Shipping Weight ..... 7.0 lbs. (3.2 kg)

#### Heat Dissipation

25 watts typical

29 watts maximum

Max Acoustic Output: 50 DBA

### 1.2.2 Reliability Specifications:

MTBF ..... 11,000 POH, typical usage

PM ..... Not Required

MTTR ..... 30 minutes

Component Design Life ..... 5 years

#### Error Rates:

Soft read errors ..... 1 per 10<sup>10</sup> bits read

Hard read errors\* ..... 1 per 10<sup>12</sup> bits read

Seek errors ..... 1 per 10<sup>6</sup> seek

\* Not recoverable within 16 retries

## 1.2.3 Performance Specifications:

ST-506

ST-412

### Capacity

#### Unformatted

Per Drive

6.38 Megabytes

12.76 Megabytes

Per Surface

1.59 Megabytes

3.19 Megabytes

Per Track

10416 Bytes

10416 Bytes

#### Formatted

Per Drive

5.0 Megabytes

10.0 Megabytes

Per Surface

1.25 Megabytes

2.5 Megabytes

Per Track

8192 Bytes

8192 Bytes

Per Sector

256 Bytes

256 Bytes

Sectors Per Track

32

32

### Transfer Rate

5.0 Mbits/sec

5.0Mbits/sec

### Access Time

Track to Track

3ms

3ms

Average

85ms\*

85ms\*\*

Maximum

205ms\*

205ms\*\*

Setting Time

15ms

15ms

\*using fast seek algorithm (including setting)

\*\*using burst mode (including settling)

### Average Latency

8.33ms

## 1.2.4 Functional Specifications:

Rotational speed

3600 rpm ±1%

3600 rpm ±1%

Recording density

7690 bpi max

9074 bpi max

Flux density

7690 fci

9074 fci

Track density

255 tpi

345 tpi

Cylinders

153

306

Tracks

612

1224

R/W Heads

4

4

Discs

2

2

## 2.0 Functional Characteristics

### 2.1 General Operation:

The ST-506/412 disc drive consists of read/write and control electronics, read/write heads, track positioning actuator, media, and air filtration system. The components perform the following functions:

1. Interpret and generate control signals.
2. Position the heads over the desired track.
3. Read and write data.
4. Provide a contamination free environment.

### 2.2 Read/Write and Control Electronics

Electronics are packaged on two printed circuit boards. The primary board to which power, control and data signals are connected includes:

1. Index detection circuit.
2. Head position/actuator circuit.
3. Read/write circuits.
4. Drive up to speed circuit.
5. Head select circuit.
6. Write fault detection circuit.
7. Step motor drive circuit.
8. Drive select circuit.
9. Track zero detector circuit.

The second PCB, mounted to the sideframe under the primary board derives its power from the primary board and provides power and speed control to the spindle drive motor.

### 2.3 Drive Mechanism

A brushless DC drive motor rotates the spindle at 3600 rpm. The spindle is driven directly with no belt or pulley being used. The motor is thermally isolated from the head/disc assembly to minimize temperature rise in the sealed chamber containing the heads and discs. The motor and spindle are dynamically balanced to insure a low vibration level. A brake is used to quickly stop the spindle motor when power is removed. The head/disc assembly is shock mounted to minimize transmission of vibration through the chassis or frame.

### 2.4 Air Filtration System (Figures 1A & 1B)

The discs and read/write heads are fully enclosed in a module using an integral recirculation air system and absolute filter to maintain a clean environment. Integral to the filter is a port which also permits ambient pressure equalization without contaminate entry.

### 2.5 Positioning Mechanism (Figure 2)

The read/write heads are mounted on a ball bearing supported carriage which is positioned by a band actuator connected to the stepper motor shaft. The stepper motor is thermally isolated from the head/disc assembly to minimize temperature rise in the sealed chamber.

FIGURE 1A  
AIR FILTRATION SYSTEM

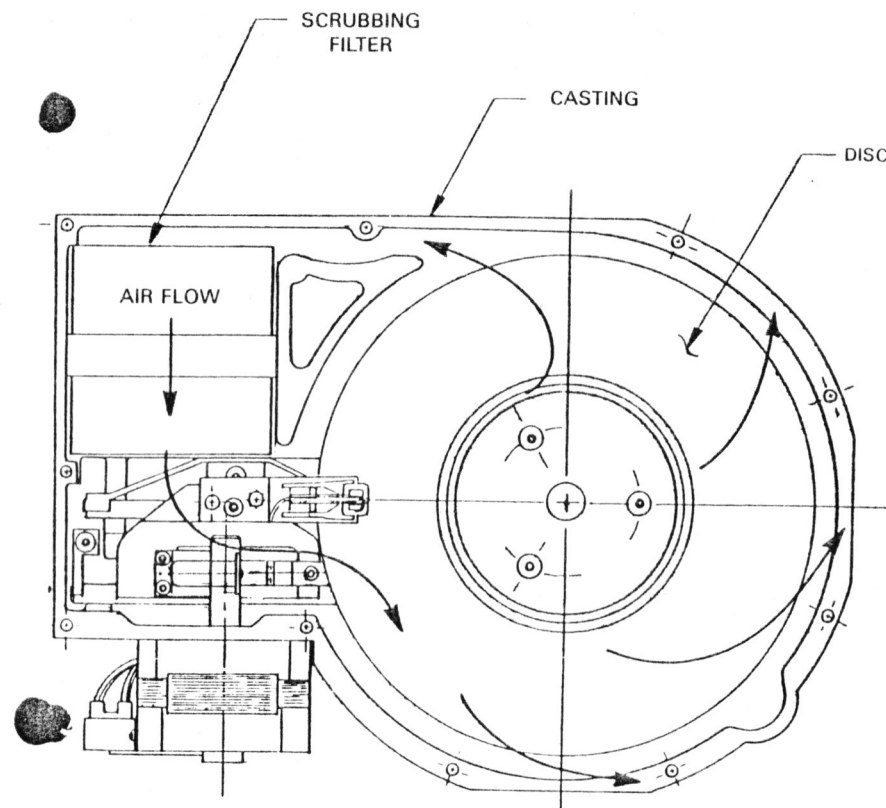


FIGURE 1B  
AIR FILTRATION SYSTEM

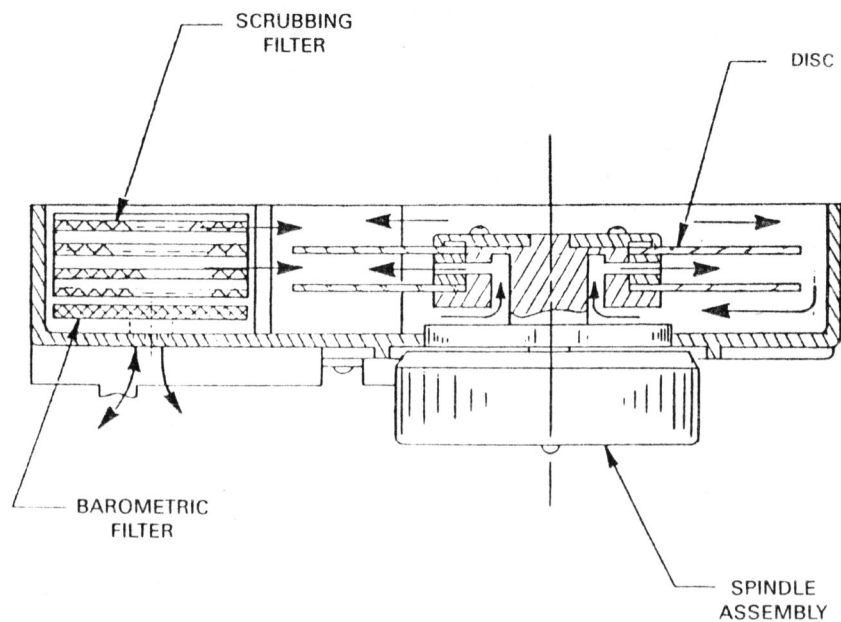
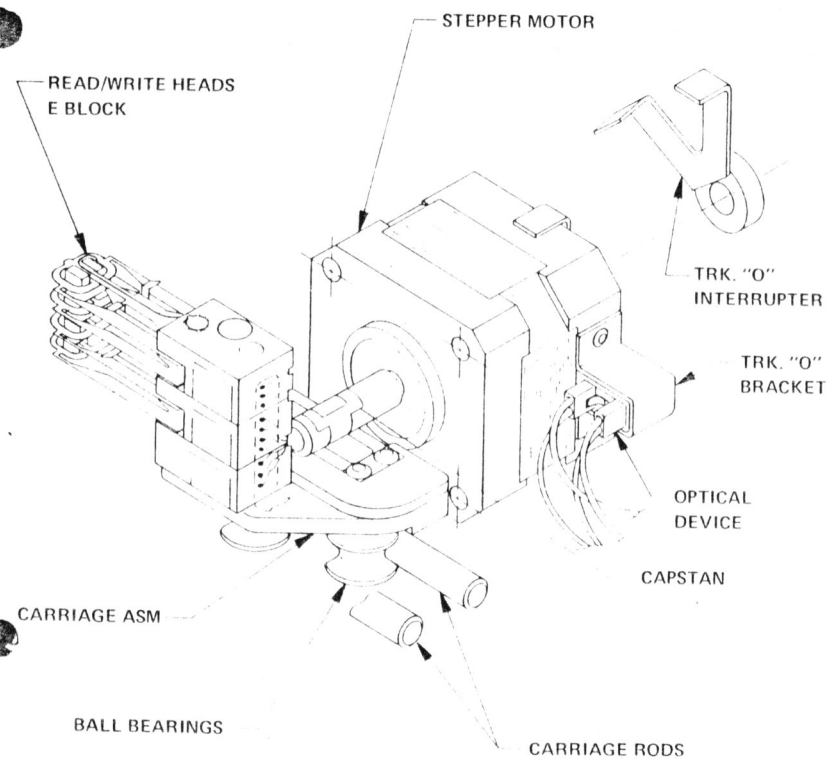


FIGURE 2  
POSITIONING MECHANISM



## 2.6 Read/Write Heads and Discs

The recording media consists of a lubricated thin magnetic oxide coating on a 130 mm diameter aluminum substrate. This coating formulation, together with the low load force/low mass flying heads, permits reliable contact start/stop operation.

Data on each of the four disc surfaces is read by one read/write head, each of which accesses 153/306 tracks.

## 3.0 Functional Operations

### 3.1 Power Sequencing (Figure 3)

Plus 5 and +12 volts may be applied in any order; however, +12 volts must be applied to start the spindle drive motor. A speed sense circuit counts 512 disc revolutions before recalibrating the heads to track 0 (See section 4.5.2 for exception). For this recalibration to occur, the step input signal must be inactive. TRACK 0, SEEK COMPLETE and READY signals on the interface will become true sequentially. The drive will not perform read, write or seek functions until READY becomes true.

### 3.2 Drive Selection

Drive selection occurs when one of the DRIVE SELECT lines is activated. Only the selected drive will respond to the input signals, and only that drive's output signals are then gated to the controller interface (See section 4.5.1 for exception).

### 3.3 Track Accessing

Read/write head positioning is accomplished by:

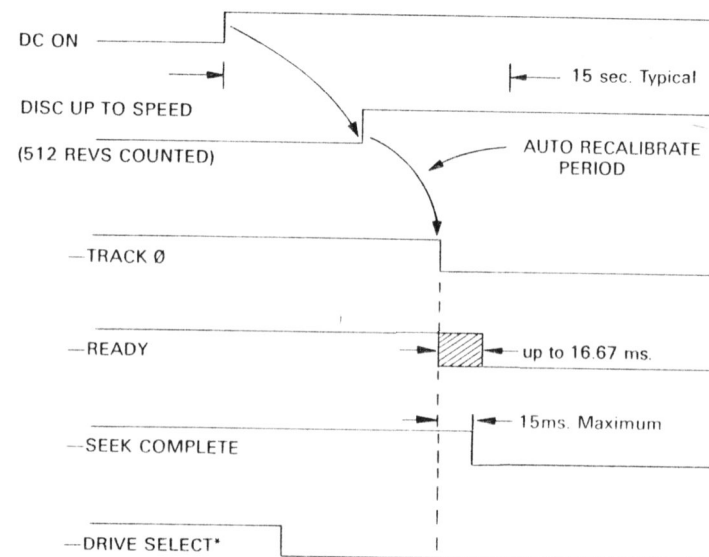
- Deactivating Write Gate.
- Activating the appropriate Drive Select line.
- Being in the READY condition with SEEK COMPLETE true.
- Selecting the appropriate direction.
- Pulsing the Step line.

Each step pulse will cause the heads to move either 1 track in or 1 track out depending on the level of the Direction line. A low level on the Direction line will cause a seek inward toward the spindle; a high, outward toward track 0.

### 3.4 Head Selection

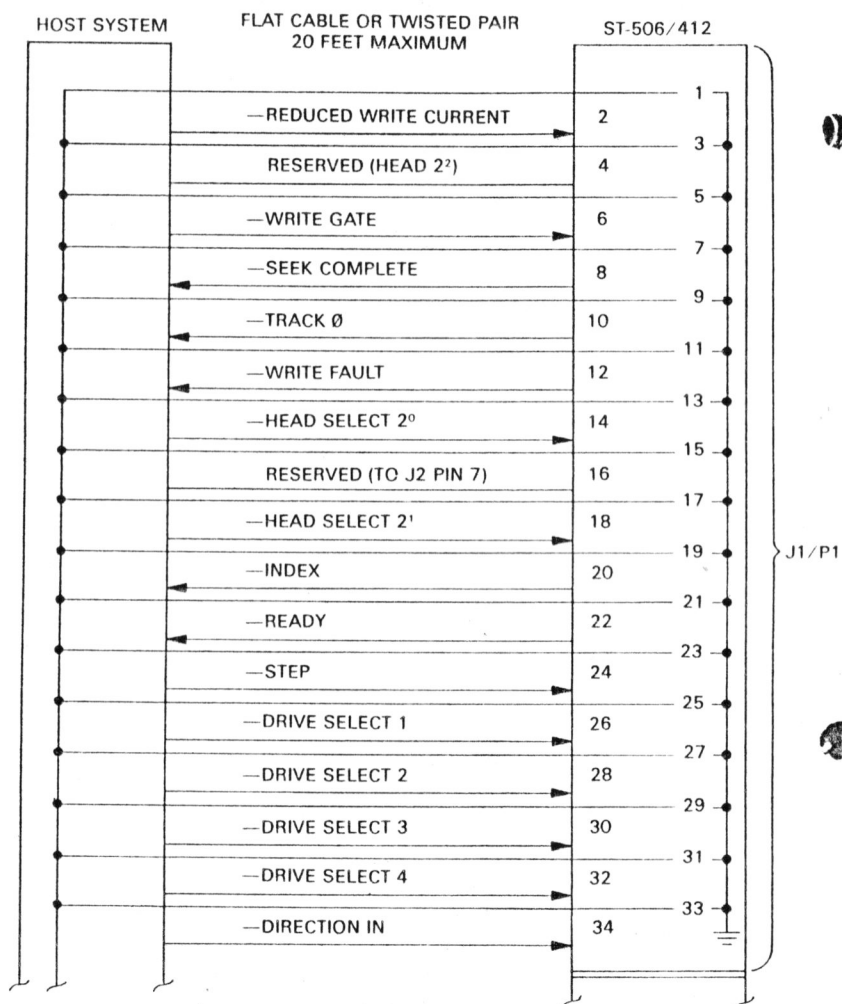
Any of the 4 heads can be selected by placing the head's binary address on the two Head Select lines.

FIGURE 3  
POWER UP SEQUENCE

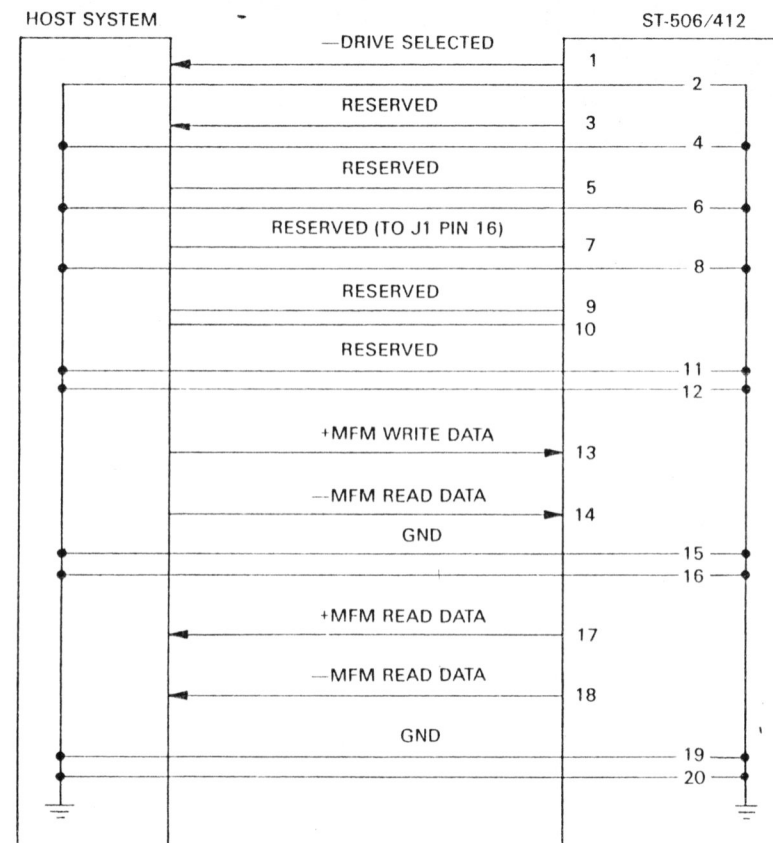


(\*GATES READY, TK 0, SEEK COMPLETE)

**FIGURE 4**  
**CONTROL SIGNALS**

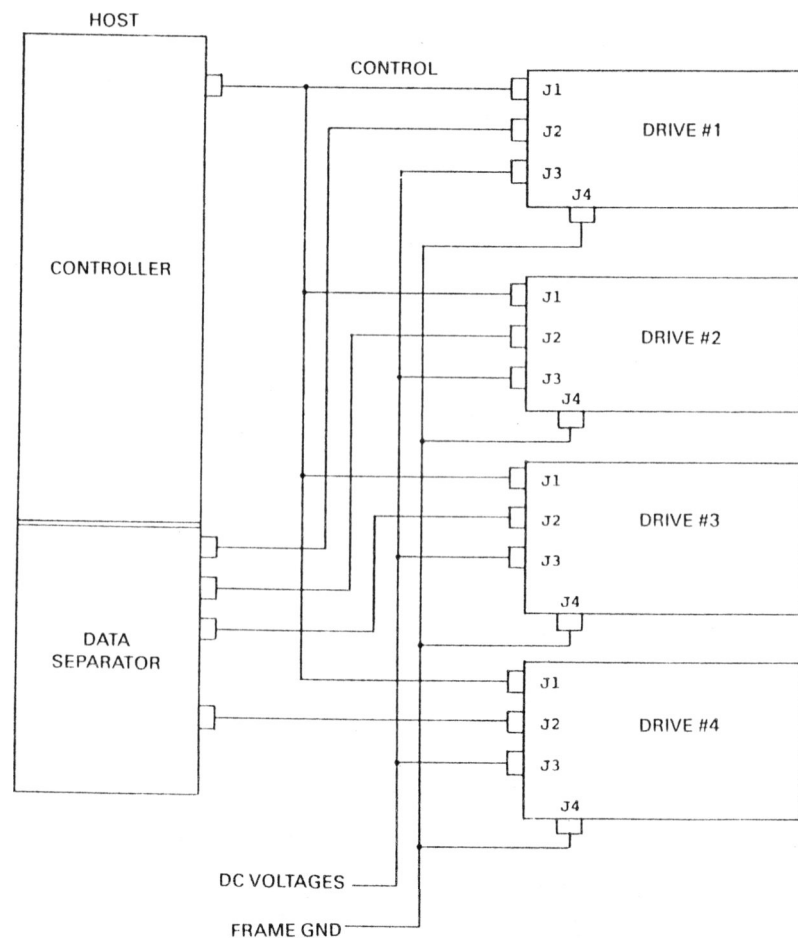


**FIGURE 5**  
**DATA SIGNALS**  
FLAT CABLE OR TWISTED PAIR  
20 FEET MAXIMUM





**FIGURE 6**  
**TYPICAL CONNECTION, 4 DRIVE SYSTEM**



#### 4.1 Control Input Lines

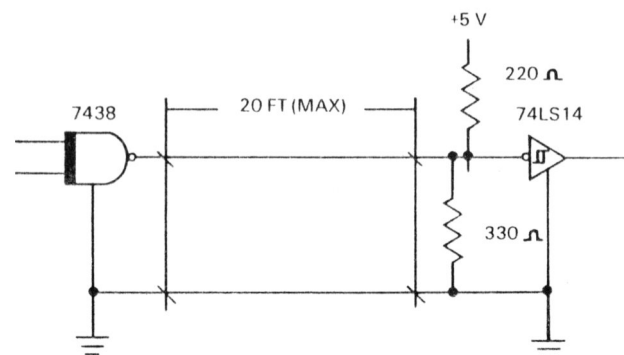
The control input signals are of two types: those to be multiplexed in a multiple drive system and those intended to do the multiplexing. The control input signals to be multiplexed are REDUCED WRITE CURRENT, WRITE GATE, HEAD SELECT 2<sup>0</sup>, HEAD SELECT 2<sup>1</sup>, STEP and DIRECTION IN. The signal to do the multiplexing is DRIVE SELECT 1, DRIVE SELECT 2, DRIVE SELECT 3 or DRIVE SELECT 4.

The input lines have the following electrical specifications. Refer to Figure 7 for the recommended circuit.

TRUE: 0.0VDC to 0.4VDC @ I = -48 mA (MAX)

FALSE: 2.5 VDC to 5.25 VDC @ I = +250  $\mu$ A (OPEN COLLECTOR)

**FIGURE 7**  
**CONTROL SIGNALS DRIVER/RECEIVER COMBINATION**



#### 4.1. Reduced Write Current (Not used on 412)

This line, when active together with WRITE GATE, causes the write circuitry to write on the disc with a lower write current. It is required that this line to be set true when writing is to be performed on cylinders 128 through 152, and set false when writing is to be performed on cylinders 0 through 127.

A 220/330 ohm resistor pack allows for line termination.

#### 4.1.2 Write Gate

The active state of this signal, or low level, enables write data to be written on the disc. The inactive state of this signal, or high level, enables data to be transferred from the drive.

A 220/330 ohm resistor pack allows for line termination.

#### 4.1.3 Head Select 2<sup>0</sup> and 2<sup>1</sup>

These two lines allow selection of each individual read/write head in a binary coded sequence. HEAD SELECT 2<sup>0</sup> is the least significant line. Heads are numbered 0 through 3. When both HEAD SELECT lines are high (inactive), head 0 will be selected.

A 220/330 ohm resistor pack allows for line termination.

#### 4.1.4 Direction In

This signal defines direction of motion of the R/W head when the STEP line is pulsed. An open circuit or high level defines the direction as "out" and if a pulse is applied to the STEP line, the R/W heads will move away from the center of the disc. If this line is a low level, the direction of motion is defined as "in" and the R/W heads will move toward the center of the disc. Change in direction must meet the requirement shown in Figure 8.

A 220/330 ohm resistor pack allows for line termination.

**Note:** Direction must not change during step time.

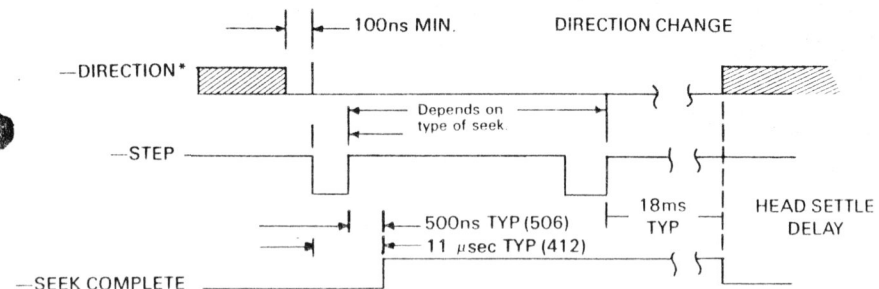
#### 4.1.5 Step

This interface line is a control signal which causes the R/W head to move in the direction of motion defined by the DIRECTION IN line.

The access motion is initiated at the low to high level transition or trailing edge of the signal pulse. Any change in the DIRECTION line must be made at least 100ns before the leading edge of the step pulse (refer Figure 8A for general timing requirements).

A 220/330 resistor pack allows for line termination.

**FIGURE 8A  
SEEK TIMING GENERAL**

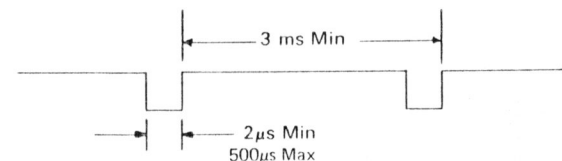


\*Change in direction can not be made prior to seek complete.

#### Slow Seek (506 and 412)

The R/W head will move at the rate of the incoming step pulses. The minimum time between successive steps is 3.0ms. The minimum pulse width is 2.0 μsec. See Figures 8A and 8B for step timing.

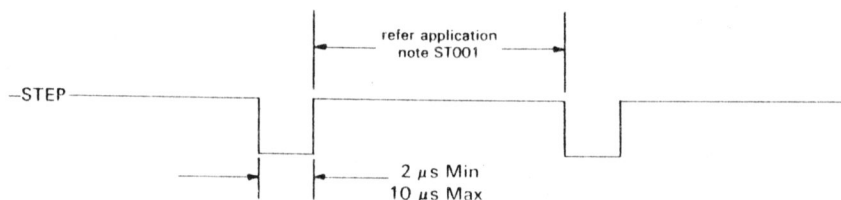
**FIGURE 8B  
SLOW SEEK STEP PULSE TIMING**



#### Algorithm Driven Seek (Not supported on 412)

In order to better utilize the stepper motor's speed characteristics, the controller can issue step pulses at a rate faster than 3ms. This algorithm accelerates the motor to its maximum speed, steps it slightly less than the desired distance, and then decelerates it prior to arriving on the specified track. Employing this algorithm allows access time to be reduced considerably while maintaining a 15ms setting time. For more information consult Seagate Application Note ST001.

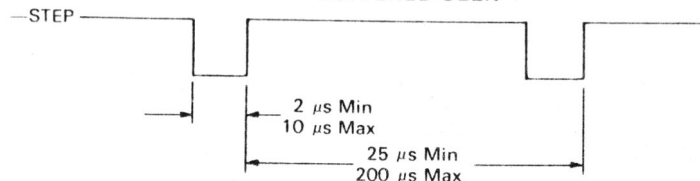
**FIGURE 8C**  
**ALGORITHM DRIVEN SEEK**



#### Buffered Seek (ST-412only)

Microprocessor utilization on the ST412 adds the capability of capturing and storing up to 305 step pulses. The controller may burst pulses to the 412 and they will be accepted until 1) time after last pulse exceeds 200 usec or 2) 305 step pulses are received. At the occurrence of either of these conditions, the ST412 microprocessor will stop accepting step pulses from the controller and will begin issuing them to the stepper motor. Depending on the length of seek, the microprocessor will select the optimum algorithm. Any pulses issued at a rate between 200 usec and 3 msec may be lost (refer Figures 8A & 8D).

**FIGURE 8D**  
**BUFFERED SEEK**



#### 4.1.6 DRIVE SELECT 1—4 (Figure 13)

DRIVE SELECT, when a low level, connects the drive interface to the control lines. Cutting the appropriate shunts at IC position 6B (6E on 412) will determine which select line on the interface will activate that drive. The following table indicates which DRIVE SELECT shunts must be cut.

DRIVE SELECT	CUT SHUNTS
DS 1	10-7, 11-6, and 12-5
DS 2	9-8, 11-6, and 12-5
DS 3	9-8, 10-7, and 12-5
DS 4	9-8, 10-7, and 11-6

#### 4.2 CONTROL OUTPUT LINES

The output control signals are driven with an open collector output stage capable of sinking a maximum of 48mA at low level or true state with maximum voltage of 0.4V measured at the driver. When the line driver is in the high level or false state, the driver transistor is off and the collector leakage current is a maximum of 250uA.

All J1 output lines are enabled by their respective DRIVE SELECT line.

Figure 7 shows the recommended circuit.

##### 4.2.1 SEEK COMPLETE<sub>E</sub>

This line will go to a low level or true state when the R/W heads have settled on the final track at the end of a seek. Reading or writing should not be attempted when seek complete is false.

SEEK COMPLETE will go false in three cases:

- 1) A recalibration sequence is initiated (by drive logic), at power on, if the R/W heads are not over track zero.
- 2) 500ns (typical) after the leading edge of a step pulse or series of step pulses.
- 3) If +5 volts or +12 volts are lost momentarily but restored.

##### 4.2.2 TRACK 0

This interface signal indicates a low level or true state only when the drive's R/W heads are positioned at cylinder zero (the outermost data track).

##### 4.2.3 WRITE FAULT

This signal is used to indicate a condition exists at the drive that may cause improper writing on the disc. When this line is a low level or true, further writing and stepping is inhibited at the drive until the condition is corrected. Write fault cannot be reset via the interface.

Note: controller should edge detect this signal.

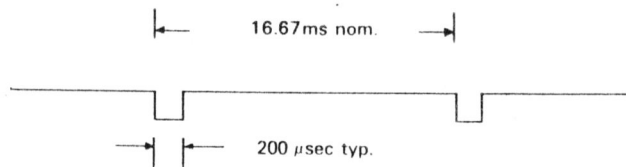
There are three conditions detected:

- a) Write current in a head without WRITE GATE active or no write current with WRITE GATE active and DRIVE SELECTED.
- b) Multiple heads selected, no head selected, or improperly selected.
- c) DC voltages are grossly out of tolerance.

#### 4.2.4 INDEX (Figure 9)

This interface signal is provided by the drive once each revolution (16.67ms nom.) to indicate the beginning of a track. Normally, this signal is a high level and makes the transition to a low level to indicate INDEX. Only the transition from high to low is valid.

**FIGURE 9  
INDEX TIMING**



#### 4.2.5 READY

This interface signal when true together with SEEK COMPLETE, indicates that the drive is ready to read, write or seek, and that the I/O signals are valid. When this line is false, all writing and seeking is inhibited.

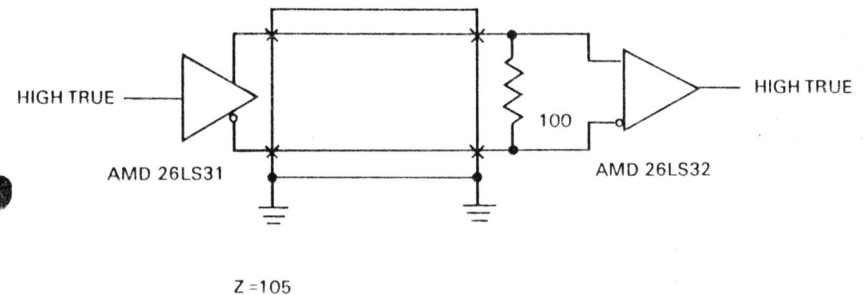
The typical time after power on for READY to be true is 15 seconds.

#### 4.3 DATA TRANSFER LINES

All lines associated with the transfer of data between the drive and the host system are differential in nature and may not be multiplexed. These lines are provided at the J2/P2 connectors on all drives.

Two pair of balanced signals are used for the transfer of data: WRITE DATA and READ DATA. Figure 10 illustrates the driver/receiver combination used in the drive for data transfer signals.

**FIGURE 10  
DATA LINE DRIVER/RECEIVER COMBINATION**



FLAT RIBBON OR TWISTED PAIR  
MAXIMUM 20 FEET

NOTE: ANY EIA RS 422 DRIVER/RECEIVER PAIR WILL INTERFACE.

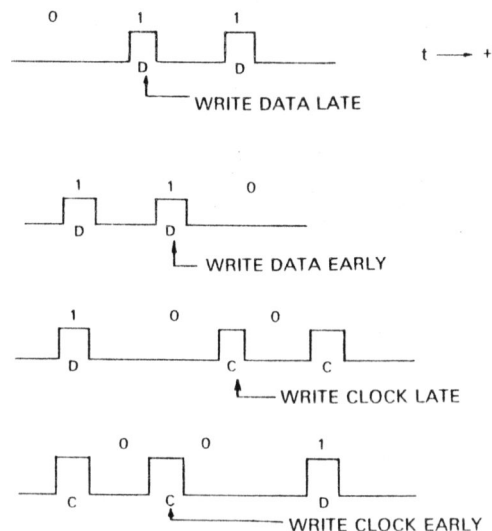
#### 4.3.1 MFM WRITE DATA

This is a differential pair that defines the transitions to be written on the track. The transition of +MFM WRITE DATA line going more positive than the -MFM WRITE DATA will cause a flux reversal on the track provided WRITE GATE is active. This signal must be driven to an inactive state (+MFM WRITE DATA more negative than -MFM WRITE DATA) by the host system when in a read mode.

To insure data integrity at the error rate specified when using an ST506, the write data presented by the host must be pre-compensated on tracks 128/128 through 152/306.

The optimum amount of pre-compensation is 12ns for both early and late written bits. Figure 11 shows the bit patterns to be compensated. All other patterns are written "on time."

**FIGURE 11**  
**WRITE PRECOMPENSATION PATTERNS**



Writing should occur out of a shift register which is used to observe the pattern. "On time" represents a nominal delay. Early and late represent less and more delay respectively.

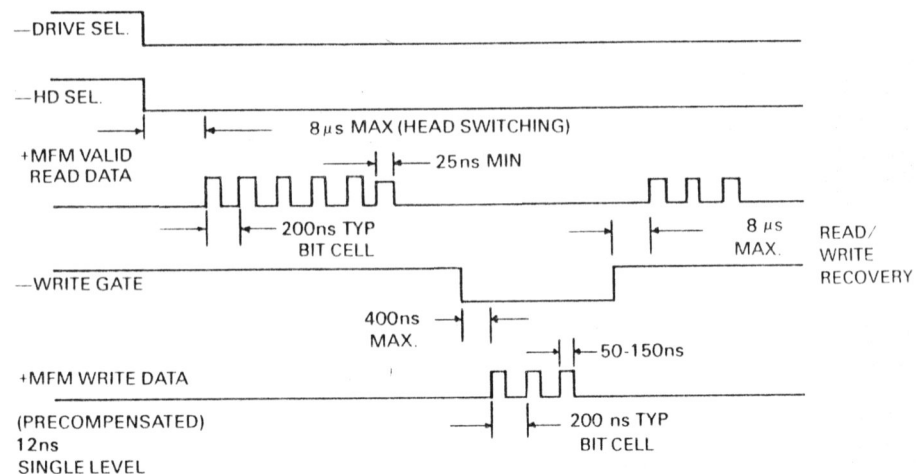
#### 4.3.2 MFM READ DATA

The data recovered by reading a pre-recorded track is transmitted to the host system via the differential pair of MFM Read Data lines. The transition of the +MFM READ DATA line going more positive than the -MFM READ DATA line represents a flux reversal on the track of the selected head.

#### 4.3.3 READ/WRITE TIMING

The timing diagram as shown in Figure 12 depicts the necessary sequence of events (with associated timing restrictions) for proper read/write operation of the drive.

**FIGURE 12**  
**READ/WRITE DATA TIMINGS**



#### 4.4 DRIVE SELECTED

A status line is provided at the J2/P2 connector to inform the host system of the selection status of the drive.

The DRIVE SELECTED line is driven by a TTL open collector driver as shown in Figure 7. This signal will go active only when the drive is programmed as drive x (x= 1,2,3, or 4) by cutting the shunt on the drive. The DRIVE SELECT X line at J1/P1 is activated by the host system.

#### 4.5 CUSTOMER OPTIONS (Figure 13)

Three optional features which are implemented via a shunt block at IC position 6B (6E on the 412) on the main printed circuit board are available for customer reconfiguration of the drive functions.

##### 4.5.1 "R" (Radial) Option

As shipped, the 14 pin shunt block (16 pin socket) is plugged in pins 2-15, leaving pins 1 and 16 open. This results in a daisy chain operation. Outputs are not active until the drive is selected. Moving the shunt block one position, to use pins 1 and 16, results in radial operation. In this case, all output signals are active, even if the drive is not selected. However, in this case, the front panel LED will not be on. Drive Select must be active to light the LED.

##### 4.5.2 "D" (Defeat Recal) Operation \*

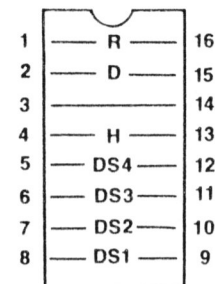
As shipped, the "D" shunt, pins 2-15, is shorted. In this case, whenever a power up sequence is performed, the heads will automatically be repositioned to track 0. Cutting the shunt D will defeat the automatic recal operation, allowing the drive to become "Ready" earlier. However, during power up, the stepper circuitry will always put phase "A" active. Thus, there is no guarantee that the drive heads will be positioned at the same cylinder as existed when the drive was powered down. It will start at the same track only if the track corresponded to one which utilizes phase A. When using this option, issuing a Read ID command would allow determination of the active address, and could be used to initialize a present track address register.

##### 4.5.3 "H" (Half Step) Option (on 412 this line is unused)

As shipped, the "H" shunt, pins 4-13, is shorted. In this case step pulses are applied to the interface at an interval of 3 milliseconds as shown in Figure 8A. Cutting shunt "H" allows a significant decrease in access time when used in conjunction with a simple software algorithm supplied by the user (refer Figure 8C). For detailed implementation information, contact the factory for a copy of Application Note ST-001 (ST Part Number 36001-001).

\*ST412 will continually seek from TK0-305 if this jumper is cut.

FIGURE 13  
OPTION SHUNT BLOCK



DS1, DS2, DS3, DS4 = Drive Selected

H = Half Step Option

D = Defeat Auto Recal

R = Radial Connection

Note: Jumper shorted is active condition for DS1, DS2, DS3, DS4, and R.  
Jumper open is active condition for H and D.

## 5.0 Physical Interface:

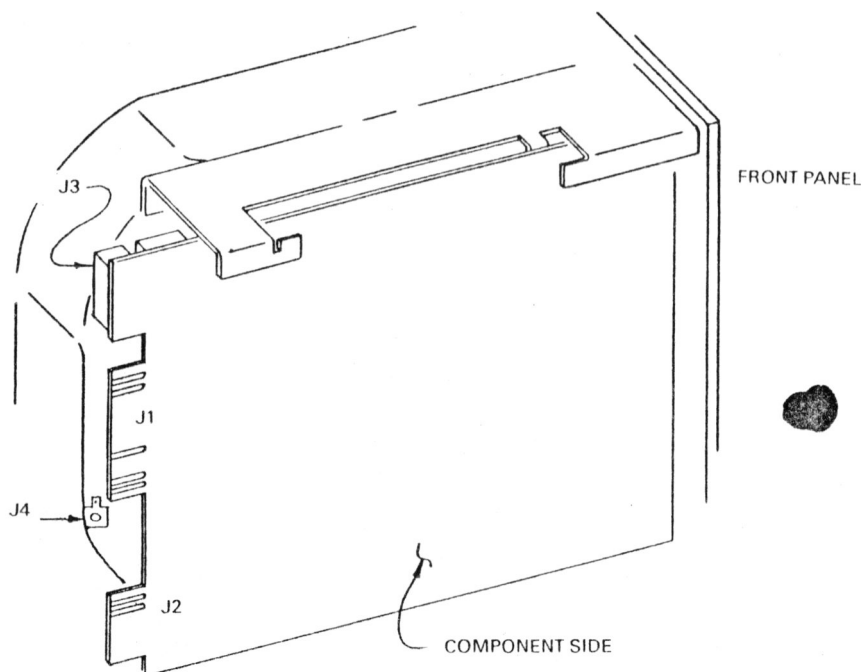
The electrical interface between the ST506/412. and the host controller is via four connectors:

1. J1 - Control signals (multiplexed)
2. J2 - Read/write signals (radial)
3. J3 - DC power input
4. J4 - Frame ground

Refer to Figure 14 for connector locations.

FIGURE 14

## INTERFACE CONNECTOR PHYSICAL LOCATIONS



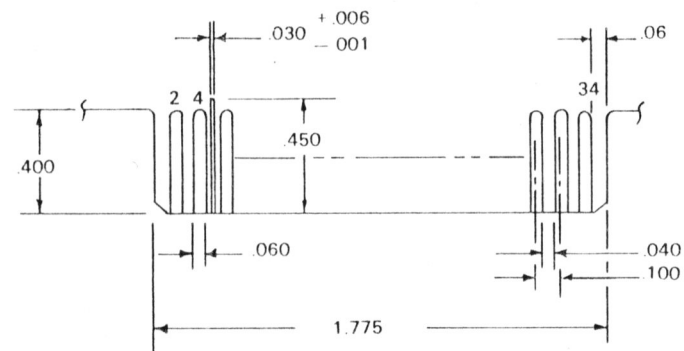
### 5.1 J1/P1 Connector—Control Signals

Connection of J1 is through a 34 pin edge connector. The dimensions for this connector are shown in Figure 15. The pins are numbered 1 through 34 with the even pins located on the component side of the PCB. Pin 2 is located on the end of the PCB connector closest to the DC Power connector J3/P3 and is labelled. The recommended mating connector for P1 is AMP ribbon connector P/N88373-3 or Molex 15-35-1341. All odd pins are ground.

A key slot is provided between pins 4 and 6.

FIGURE 15

### J1 CONNECTOR DIMENSIONS



Unless noted, .xx =  $\pm .030$ , .xxx =  $\pm .010$

BOARD THICKNESS  
.062 + .007

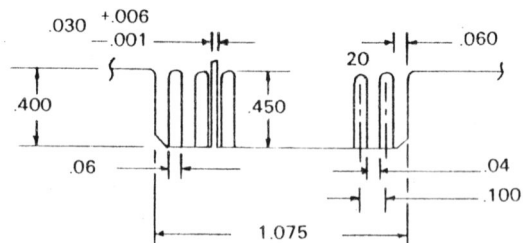
Current requirements and connector pin numbers are shown in Table IV.

## 5.2 J2/P2 Connector—Data Signals

Connection to J2 is through a 20 pin edge connector. The dimensions for the connector are shown in Figure 16. The pins are numbered 1 through 20 with the even pins located on the component side of the PCB. The recommended mating connector for P2 is AMP ribbon connector P/N 88373-6, or Molex P/N 15-35-1201.

A key slot is provided between pins 4 and 6.

**FIGURE 16**  
**J2 CONNECTOR DIMENSIONS**



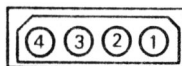
BOARD THICKNESS  
.062 ± .007

Unless Noted:  
.xx = +.030  
.xxx = .010

## 5.3 J3/P3 Connector—DC Power

DC power connector (J3) is a 4 pin AMP Mate-N-Lok connector P/N 350211-1 mounted on the solder side of the PCB. The recommended mating connector (P3) is AMP P/N 1-408424-0 utilizing AMP pins P/N 350078-4 (Strip) or P/N 61173-4 (Loose Piece). J3 pins are numbered as shown in Figure 17.

**FIGURE 17**  
**J3 CONNECTOR—DRIVE PCB SOLDER SIDE**



**TABLE IV**

**DC POWER REQUIREMENTS**

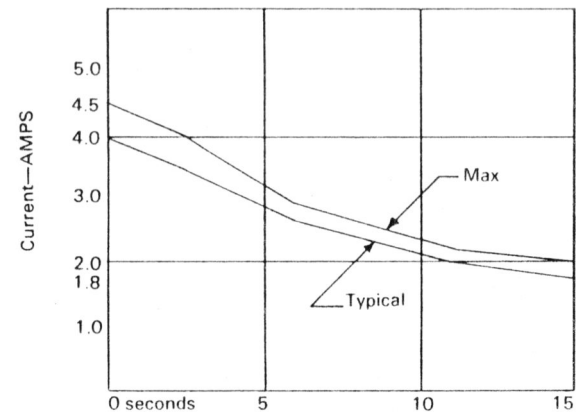
J3 Connector	Current AMPS	
	Max	Typ
Pin 4 +5 Volts DC ± 5% Pin 3 +5 Volt Return	1.0	0.7
Pin 1 +12 Volts DC ± 5%* Pin 2 +12 Volt Return	4.5**	1.8

\* ±10% at power on or seeking, ±5% for reading or writing.

\*\* Occurs only during power up, per curve below.

**TABLE V**

**MOTOR START CURRENT REQUIREMENTS**



+12V current power up cycle



#### 5.4 J4/P4 Frame Ground Connector

Faston AMP P/N 61761-2

Recommended mating connector AMP 62187-1

If used, the hole in J4 will accommodate a wire size of 18 AWG max.

#### 6.0 Physical Specifications

This section describes the mechanical dimensions and mounting recommendations for the ST-506/412

##### 6.1 Mounting Orientation

Recommended orientation is either vertical on either side or horizontal with PCB down. The only prohibited orientation is horizontal with PCB up. *In the final mounting configuration, insure that operation of the four shock mounting screws should not protrude inside the frame more than .09 inches.*

##### 6.2 Mounting Holes

Eight mounting holes, four on the bottom and two on each side are provided for mounting the drive in an enclosure. The size and location of these holes, shown in Figure 18, are identical to the industry standard minifloppy drive.

##### 6.3 Physical Dimensions

Overall height/width/depth and other key dimensions are shown in Figures 18 and 19. As in the case of the mounting holes, the dimensions are identical to the minifloppy, allowing a direct physical replacement.

##### 6.4 Shipping Requirement

For shipping the heads are positioned over track 140/280 and are held to approximately that position by an edge rubber placed on the top cover. By securing the heads in this manner, there is enough free travel to insure that the heads do not absorb the total shock of any impact, while preventing them from hitting the crash stops. The edge rubber should be removed for use and is not necessary when the drive is shipped mounted in a system. No other precautions are required when shipping the drive.

FIGURE 18  
MOUNTING PHYSICAL DIMENSIONS

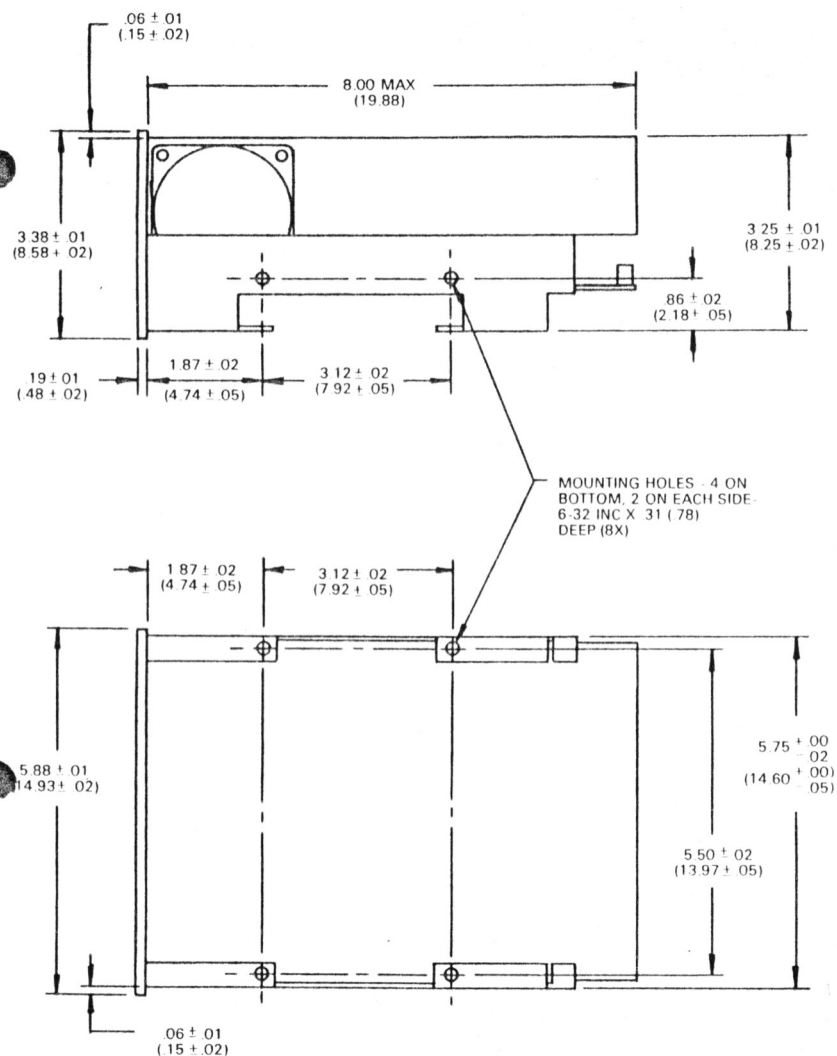
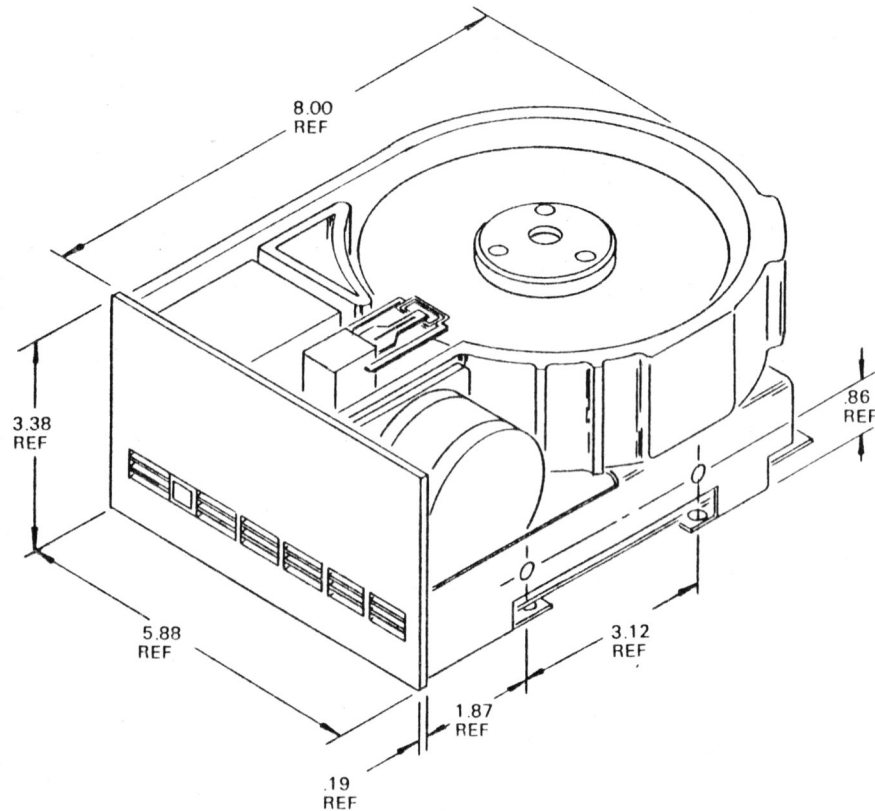


FIGURE 19

OVERALL PHYSICAL DIMENSIONS



7.0 Track Format

The purpose of a format is to organize a data track into smaller sequentially numbered blocks of data called sectors. The format is a soft sector type which means that the beginning of each sector is defined by a prewritten identification (ID) field which contains the physical sector address plus cylinder and head information. The ID field is then followed by a user supplied data field.

The format is a slightly modified version of the IBM System 34 double density format which is commonly used on floppy disc drives. The encoding method is Modified Frequency Modulation (MFM).

Figure 20 shows the track format as shipped. 8192 bytes are available on each track, based on 32 sectors, each having 256 bytes of user data.

The beginnings of both the ID field and the data field are flagged by unique characters called address marks. An address mark is two bytes in length. The first byte is an "A1" data pattern. This is followed by either an "FE" pattern for an ID address mark, or an "F8" pattern for the data address mark.

The "A1" pattern is made unique by violating the encoding rules of MFM by omitting one clock bit. This makes the address mark pattern unique to any other serial bit combination that could occur on the track. See Figure 21 depiction of the "A1" byte. Each ID and data field is followed by a 16 bit cyclic redundancy check (CRC) character used for a particular data pattern.

Surrounding the ID and data fields are gaps to establish physical and timing relationships between these fields.

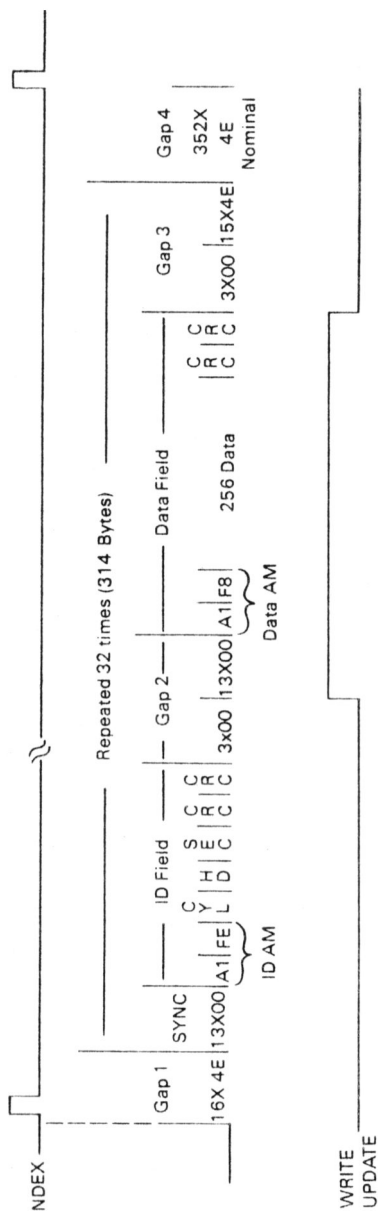
7.1 Gap 1

Gap 1 is to provide for variations in Index detection. As shipped, gap 1 is 16 bytes long, but must be at least 12 bytes. Gap 1 is immediately followed by a sync field preceding the first ID field.

7.2 Gap 2

Gap 2 follows the CRC bytes of the ID field, and continues to the data field address mark. It provides a known area for the data field write splice to occur. The latter portion of this gap serves as the sync up area for the data field AM. As shipped gap 2 is 16 bytes. Minimum length required is determined by the "lock up" performance of the phase-lock-loop in the data separator, which is part of the host control unit.

FIGURE 20  
TRACK FORMAT AS SHIPPED



**NOTES:** 1. Nominal Track Capacity = 10416 Bytes

2. Total Data Bytes/Track =  $256 \times 32 = 8,192$

3. Sector interleave factor is 4. Sequential ID Fields are sector numbered 0, 8, 16, 24, 1, 9, 17, 25, 2, 10, 18, 26, etc.

4. Data Fields contain the bit pattern 0000 as shipped

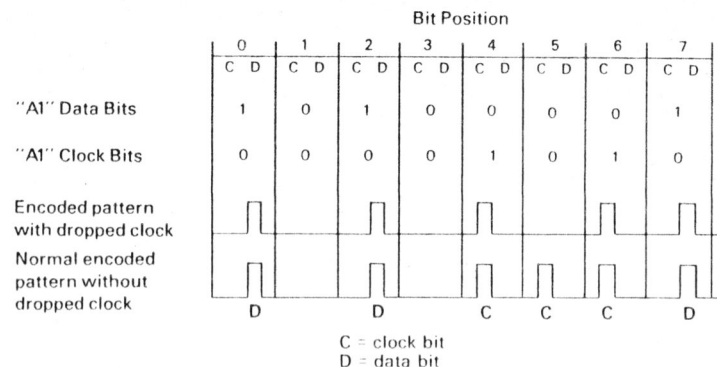
5. CRC Fire Code =  $x^{15} + x^{12} + x^5 + 1$

6. Bit 7 of Head Byte ID Field equals 1 in a defective sector (Cylinder 0 is error free)

7. Bit 5 of Head Byte reserved for numbering cylinders greater than 256

8. Bit 6 of Head Byte reserved for numbering cylinders greater than 512

FIGURE 21  
"A1" ADDRESS MARK BYTE



7.3 Gap 3

Gap 3 following each data field allows for the spindle speed variations. This allows for the situation where a track has been formatted while the disc is running faster than nominal, then write updated with the disc running slower than normal. Without this gap, or if it is too small, the sync bytes or ID field of the next field of the next field could be over written. As shipped, the gap allows a  $\pm 3\%$  speed variation (actual drive spec is  $\pm 1\%$ ). Minimum gap is 8 bytes for a 256 byte record size.

7.4 Gap 4

Gap 4 is a speed tolerance buffer for the entire track, which is applicable in full track formatting operations to avoid overflow into the index area. The format operation which writes ID fields begins with the first encountered index and continues to the next index. The actual bytes in Gap 4 depends on the exact rotating speed during the format operation.

7.5 Sector Interleaving

As shipped, the track format uses an interleave factor of 4. That is sequentially sector ID numbers are 0, 8, 16, 24, 1, 9, 17, 25, 2, 10, 18, 26, etc. This allows sufficient system turnaround time to process multiple sectors during a single revolution, thus enhancing through-put of typical file read/write operations.

7.6 Defective Sector Flags

As shipped, any sector which is considered marginal for data recording or which has a permanent defect, will be indicated by the presence of a 1 in bit position 7 of the head byte in the ID field.

In addition, a printout will be provided with each drive which lists the location of these same defects in terms of head number, cylinder number, sector and byte.

No units will be shipped to customers if surface analysis identifies more than 3 hard errors per surface, or 8 total errors per drive. Additionally no errors will be present on cylinder 0

Testing for defects involves an analysis of the total media surface under marginalized test conditions.